MoSys, Inc.
Form 10-K
March 12, 2019
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UNITED STATES

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
For the Fiscal Year December 31, 2018 or

TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
Commission file number: 000-32929

MOSYS, INC.

(Exact name of registrant as specified in its charter)

Delaware	77-0291941
(State or other jurisdiction of incorporation or organization)	(IRS Employer Identification Number)
2309 Bering Drive	
San Jose, California 95131	
(Address of principal executive offices)	

(408) 418-7500

(Registrant’s telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	Name of each exchange on which registered
Common Stock, par value $0.001 per share	Capital Market of the NASDAQ

Stock Market, LLC

Securities registered pursuant to Section 12(g) of the Act:

Title of each class	Name of each exchange on which registered
Series AA Preferred Stock, par value $0.01 per share	None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes No

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes No

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes No

Indicate by check mark whether the registrant has submitted electronically every Interactive Data File required to be submitted pursuant to Rule 405 of Regulation S-T (§232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit such files). Yes No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§ 229.405 of this chapter) is not contained herein, and will not be contained, to the best of registrant’s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, a smaller reporting company, or emerging growth company. See the definitions of “large accelerated filer,” “accelerated filer,” “smaller reporting company,” and "emerging growth company" in Rule 12b-2 of the Exchange Act:

Large accelerated filer	Accelerated filer
Non-accelerated filer	Smaller reporting company
Emerging Growth Company	

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act.

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes No

The aggregate market value of the common stock held by non-affiliates of the registrant, as of June 30, 2018 was $13,947,204 based upon the last sale price reported for such date on the Capital Market of the NASDAQ Stock Market. For purposes of this disclosure, shares of common stock held by the Registrant and beneficial owners of more than 5% of the outstanding shares of common stock who the Registrant believes may be affiliates, if any, have been excluded as shares that might be deemed to be held by affiliates. The determination of affiliate status for this purpose is not necessarily a conclusive determination for any other purpose.

As of February 28, 2019, 43,121,730 shares of the registrant's common stock, $0.001 par value per share, were outstanding.

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ANNUAL REPORT ON FORM 10-K

FOR THE YEAR ENDED DECEMBER 31, 2018

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Part I

This Annual Report on Form 10-K and the documents incorporated herein by reference contain forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, which include, without limitation, statements about the market for our products, technology, our strategy, competition, expected financial performance and other aspects of our business identified in this Annual Report, as well as other reports that we file from time to time with the Securities and Exchange Commission. Any statements about our business, financial results, financial condition and operations contained in this Annual Report that are not statements of historical fact may be deemed to be forward- looking statements. Without limiting the foregoing, the words “believes,” “anticipates,” “expects,” “intends,” “plans,” “projects,” or similar expressions are intended to identify forward-looking statements. Our actual results could differ materially from those expressed or implied by these forward-looking statements as a result of various factors, including the risk factors described in Part I., Item 1A, “Risk Factors,” and elsewhere in this report. We undertake no obligation to update publicly any forward-looking statements for any reason, except as required by law, even as new information becomes available or other events occur in the future.

MoSys®,1T-SRAM®, Bandwidth Engine® and GigaChip® are registered trademarks of MoSys, Inc. LineSpeed™ is a trademark of MoSys, Inc.

Item 1. Business

Overview

MoSys, Inc., together with its subsidiaries (“MoSys,” the “Company,” “we,” “our” or “us”), is a fabless semiconductor compar focused on the development and sale of integrated circuits, or ICs, for the high-speed cloud networking, communications, security appliance, video, monitor and test, data center and computing markets. Our solutions deliver time-to-market, performance, power, area and economic benefits for system original equipment manufacturers, or OEMs. Our primary product line is marketed under the Blazar Accelerator Engine name and comprises our Bandwidth Engine and Programmable HyperSpeed Engine, or PHE, IC products, which integrate our proprietary, 1T-SRAM high-density embedded memory and a highly-efficient serial interface protocol resulting in a monolithic memory IC solution optimized for memory bandwidth and transaction access performance. Further performance benefits can be achieved to offload statistical, search or other custom functions using our optional integrated logic and processor elements. As data rates and the amount of high-speed processing increase, critical memory access bottlenecks occur. Our Bandwidth Engine and PHE ICs dramatically increase memory accesses per second, removing these bottlenecks. In addition, the serial interface and high-memory capacity reduce the board footprint, number of pins and complexity, while using less power. Our LineSpeed IC product line comprises non-memory, high-speed serialization-deserialization interface, or SerDes I/O, physical layer, or PHY, devices that ensure signal integrity between interfaces which is commonly referred to as clock data recovery, or CDR, or retimer functionality, which perform multiplexing to transition from one speed to another, commonly referred to as Gearbox functionality. These PHY devices reside within optical modules and networking equipment line cards designed for next-generation Ethernet and optical transport network applications.

Industry Background

The amount of data and the number of data consumers and devices is growing exponentially, driven primarily by commercial and consumer cloud applications, video services, high speed mobile networks, Internet of Things, or IoT, and many other cloud applications. In order to meet these demands, the new cloud infrastructure, including the

backbone, edge, access network and data centers, must scale in both speed and intelligence to handle real-time security, bandwidth allocation, and service-level expectations. In addition, workloads or applications delivered at a massive scale from the cloud require flexible and efficient data transmission to optimize resources to enable these applications and lower the overall cost, size and power of the data center. These increased demands strain communication between onboard IC devices, limiting the data throughput in network switches and routers and the network backbone.

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To meet these demands, carrier and enterprise networks are merging with the cloud and are undergoing significant changes and, most significantly, are migrating to packet-based Ethernet networks that enable higher throughput, lower cost and uniform technology across access, core and metro network infrastructure. These networks are now being designed to deliver voice, video and high-speed Internet services on one converged, efficient and flexible network. These trends require networking systems, especially the high-speed switches, security appliances and routers that primarily comprise these networks, to comply with evolving market requirements and be capable of providing new services and better quality of service while supporting new protocols and standards. To support these trends, traditional OEM network and telecommunications equipment manufacturers, such as Nokia Corporation, and its subsidiary, Alcatel-Lucent, Cisco Systems, Inc., Tel. LM Ericsson, Fujitsu Ltd., Hitachi Ltd., Huawei Technologies, and Juniper Networks, Inc., as well as new vendors and cloud-service providers, who are delivering a new set of white-box solutions, must offer higher levels of packet forwarding rates, bandwidth density and be optimized to enable higher-density, lower-power data path connectivity in the next generations of their networking systems.

Networking communications, security, video and computing systems throughout the cloud network must operate at higher speed and performance levels, and so require new generations of packet processors and improved memory subsystems to enable system performance. These systems and their component line cards generally need to support aggregate rates of 100 gigabits per second, or Gbps, and above to meet the continued growth in network traffic. Data centers and access equipment that were previously aggregating slower traffic at rates of up to 40 Gbps now are being designed to aggregate traffic at 100 Gbps, or more. The transition to 100 Gbps networks is underway, and the increase in data rates for these networks is expected to continue to grow rapidly over the coming years.

Several types of semiconductors are included on each line card, including one or more processors and multiple memory chips. These processors are complex ICs or IC chipsets that perform high-speed data or packet processing for functions, such as traffic routing, shaping, metering, billing, statistics, detection, steering, security, video processing, monitoring and workload acceleration. The line cards use various types of memory ICs to facilitate temporary packet storage and assist in the analysis and tracking of information embedded within the data flowing through the processors. After a packet enters the line card, a packet or data processor helps separate the packet into smaller pieces for rapid analysis. In a typical packet-based network for example, the data is broken up into the packet header, which contains vital information on packet destination and type, such as the Internet protocol address, and the payload, which contains the data being sent. Generally, the line card operations must occur at full data rates and typically require accessing memory ICs many times. Simultaneously, the packet’s payload, which may be substantially larger than the packet header, is also stored in memory ICs until processing is complete and the packet can re-combine and be sent to its next system destination. Within the line card, communication between the packet processor and memory ICs occurs through an interface consisting of combinations of physical pins on each type of chip. These pins are grouped together in a parallel or a serial architecture to form a pathway, called a bus, through which information is transferred from one IC to the next.

Today, the majority of physical buses that connect networking equipment and components use a parallel architecture to communicate between processors and memory ICs, which means information can travel only in one direction and in one instance at a time. As processing speeds increase, the number of pins required and the speed of the bus in a parallel architecture become a limitation on system performance and capability. In contrast, the number of connections is reduced substantially across fewer, higher-rate pins in a serial architecture, and data is transferred simultaneously in both directions. Data transfer rates are limited by the data access rates of the various ICs included on the line card, thus leading to bottlenecks when these ICs perform inadequately. In order to remove these bottlenecks and meet next-generation bandwidth requirements, the line card ICs need to support higher access rates enabled by internal memory or high-speed serial bus architectures and these more advanced interface protocols.

Most networking and communication systems sold and in operation today include line cards that process data at speeds ranging from 10 Gbps to 400 Gbps, and support many aggregated slower ports. To accommodate the substantial and growing increase in demand for networking communications and applications, networking systems manufacturers are developing and bringing to market next-generation systems that run at aggregate speeds of 400 Gbps or more with newer products scaling to tens of thousands of Gbps, or tens of terabits, per second. Applications, such as security appliances, broadcast video, compute accelerators etc. that were previously running at aggregate rates of 10G or 40G, are moving to higher aggregate rates in the 100s of gigabits. Although processor performance in applications, such as computing and networking has traditionally doubled nearly every 18 months, or even sooner,

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the performance of external high-density memory technology has generally been able to double only once every 10 years. Existing memory IC solutions built for high capacity and based on parallel interface architecture struggle to meet the access rates required to meet speeds of 100 Gbps and beyond due to system-level limitations for pin counts, power and performance. To compensate for slow external memory access, developers must either integrate larger amounts of on-chip memory and/or utilize complex system alternatives to try to work around the access-rate limitations of these memories. The additional memory and circuitry adds to IC power, size and cost and may not be feasible depending on the economics and technology used to implement the data processor. These networking and communications systems generally comprise a chassis populated by four to 16 line cards. Often, these systems are shipped to customers with only a portion of the line card slots populated, and the customer will add additional line cards to increase system performance, capacity and features.

Each line card requires a significant amount of memory to support its processing capabilities. Traditional external memory IC solutions currently used on line cards include both dynamic random access memory, or DRAM, and static random access memory, or SRAM. Line cards in networking systems use both specialized, high-performance DRAM ICs, such as reduced-latency DRAM, or RLDRAM, low-latency DRAM, or LLDRAM, and commodity DRAM, such as double data rate, or DDR ICs. The latest DDR memory is high-bandwidth memory, or HBM, provides high bandwidth, but has fundamentally slow access time. For very high access, networking systems use higher-performance SRAM, which may be integrated into the data processing IC itself depending on size, power and economics or using traditional external SRAM IC, such as quad data rate, or QDR SRAM. These memories are very fast, but are much smaller, cost more and burn more power than traditional DRAM. Substantially all of these traditional memory IC solutions use parallel interfaces, which are slower than serial interfaces. For data processing solutions, which are unable to integrate large amounts of SRAM, such as field-programmable gate arrays (FPGA), we believe the traditional external SRAMs or RLDRAMs will be increasingly challenged to meet the performance, pin count, area and power requirements as networking systems and other new security, video, and compute systems expand beyond 100 Gbps. The result is a gap between processor and memory performance. To meet the higher performance requirements being demanded by the industry, while using current components and architectural approaches, system designers must add more discrete memory ICs to the line cards and/or add more embedded memory on the packet processor. New processor and custom data processing engine ICs are being developed that integrate more SRAM to help offset the bottlenecks, but the cost to develop these custom ICs is high and there is a trade-off in cost, power and size. FPGAs offer flexibility, lower development cost and time to market but are limited in the amount of internal circuitry and the amount of integrated SRAM memory. We believe our Bandwidth Engine family of products is well suited to address memory access bottleneck challenges and provide significant performance, size, pin count and power advantages compared to traditional external memory solutions, especially for FPGA-based systems.

In order to improve performance and resolve memory bottlenecks, there is an emerging trend in which computations are performed by algorithms on the memory device in order to reduce processing time and power consumption. This trend is sometimes called in-memory compute or processor-in-memory. In order to make a flexible solution, the in-memory compute can be accomplished with arrays of reduced instruction set computer (RISC) cores on the memory device. Further performance gains can be accomplished with application-specific enhancements to the memory device’s instruction set architecture.

We have developed our ICs to synergistically address the need for high-speed data access and throughput currently confronting system designers. We expect our IC products to meet the increasing demands placed on conventional memory technology used on the line cards in high-speed systems. We believe that our products and technology are well positioned as replacements for existing IC solutions in order to support the needs of a growing number of FPGA-based data processing applications with aggregate rates greater than 100 Gbps that require high bandwidth and

high access rate to memory.

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Our Approach

We have leveraged our proprietary intellectual property, or IP, to design our IC products to help networking OEMs address the growing bottlenecks in system performance. We have incorporated critical features into our product families to accomplish this objective.

On-Chip Acceleration

One significant performance bottleneck in any network line card is the need to transfer data between discrete ICs. Many of these data-transfer operations are iterative in nature, requiring subsequent, back-to-back accesses of the memory IC by the processor IC. Our Bandwidth Engine ICs include an arithmetic logic unit, or ALU, which enables the performance of mathematical operations on data. Moving certain processing functions from the processor IC to the Bandwidth Engine IC through the use of this embedded ALU, reduces the number of processing transactions and frees the processor IC to perform other important networking or micro-processing functions.

The PHE, which we formerly called our programmable search engine, or PSE IC, takes this concept one step further by incorporating integrated RISC processors optimized for processing data structures and graphs. The processors can be programmed by the user to offload and accelerate standard and/or customized functions from the main processor thereby reducing memory transactions and data path complexity to provide improved performance and lower system latency.

High-Performance Interface

High-speed, efficient interfaces are critical building blocks to meet high data transfer rate requirements for communication between ICs on network line cards. Semiconductor companies are increasingly turning to serial interface architectures to achieve needed system performance. For example, high-performance ICs that are sold into wide markets, such as field programmable gate arrays, or FPGAs, and network processing units, NPUs, are using serial interfaces to ensure they can compete with custom designed application specific ICs, or ASICs, by matching their performance. Using serial interfaces, IC developers also are able to reduce pin count (the wired electrical pins that connect an IC to the network line card on which it is mounted) on the IC. With reducing geometries, the size of most high-performance ICs is dictated by the number of pins required, rather than the amount of logic and memory embedded in the chip. As a result, using serial interface facilitates cost reduction and reduced system power consumption, while improving the performance of both the IC itself and the overall system. While serial interfaces provide significantly enhanced performance over parallel interfaces, SerDes interfaces traditionally have had higher power consumption, which is a challenge for IC designers. Our SerDes interfaces, however, are optimized to meet our customers' signal integrity, low-power consumption and latency requirements.

We make our interface technologies compliant with industry standards so that they can interoperate with interfaces on existing ICs. In addition, we make them programmable to support multiple data rates, which allows for greater flexibility for the system designer, while lowering development and validation costs. Interoperability reduces development time, thereby reducing the overall time to market of our customers' systems.

GigaChip Interface Protocol

In addition to the physical characteristics of the serial interface, the protocol used to transmit data is also an important element that impacts speed and performance. To address this and complement our Bandwidth Engine and PHE devices, we have developed the GigaChip Interface, or GCI, which is an open-interface transport protocol optimized

for efficient chip-to-chip communications. The GCI electrical interface is compatible with the current industry standards, including 10G and 25G IEEE and OIF interface standards, to simplify electrical interoperability between devices. GCI can enable highly efficient serial chip-to-chip communications, and its transport efficiency averages 90% for the data transfers it handles. GCI is included in our ICs and is offered to customers and prospective partners on terms intended to encourage widespread adoption.

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High-Performance and High-Density Memory Architecture

The high density of our proprietary 1T-SRAM technologies stems from the use of a single-transistor, or 1T, which is similar to DRAM, with a storage cell for each bit of information. Embedded memory utilizing our 1T-SRAM technologies is typically two to three times denser than the six-transistor storage cells used by traditional SRAM, or 6T-SRAM. Embedded memory utilizing our 1T-SRAM technologies typically provides speeds essentially equal to or greater than the speeds of traditional SRAM and DRAM, particularly for larger memory sizes. Our 1T-SRAM memory designs can sustain random access cycle times of less than three nanoseconds, significantly faster than DRAM technology. Embedded memory utilizing our 1T-SRAM technologies can consume as little as one-half the active power and generate less heat than traditional SRAM when operating at the same speed. The 1T-SRAM allows us to integrate more high-performance memory using less expensive processing technology, reduces system level heat dissipation and enables reliable operation using lower-cost packaging.

Our PHE integrates RISC cores optimized for operating data stored in the PHE's memory block. The integration of the cores with memory allows system algorithms or functions to be offloaded to the device and reduces overall system-task latency and increases throughput. New algorithms or functions can be added or adjusted to the PHE device in software.

Embedded In-Memory Functions (IMF)

We have combined our high-speed memory architecture with intelligence to define an embedded memory that can execute embedded functions and algorithms internally, or "in-memory," to allow software and hardware designers acceleration options to improve the performance of their applications.

The IMFs executed within the memory architecture in our Bandwidth Engine and PHE products result in application-performance increases by reducing the number of external memory and computational operations need to accomplish the same functions using traditional memories. Also, by executing in-memory, the resources of the packet processor and other ICs on the customer's board are available to perform other functions.

Our Strategy

Our primary business objective is to be a profitable IP-rich fabless semiconductor company offering ICs that deliver unparalleled memory bandwidth and access rate performance for high-performance data processing in cloud networking, security appliances, video, test and monitoring, and data center systems. The key components of our strategic plan include the following strategies:

Target Large and Growing Markets

Our initial strategy is to target the multi-billion dollar networking, telecommunications, security appliance and data center OEM equipment markets, and we have developed products to support the growth in 100 Gbps and higher networking speeds. We are currently supporting numerous customers, with whom we have achieved design wins. We continue to actively pursue additional design wins for the use of our ICs in our target markets. We believe our design wins represent the potential for future revenue growth. With limited history to date, however, we cannot estimate how much revenue each design win is likely to generate, or how much revenue all of these (and future design wins) are likely to generate. There is no assurance that these customer designs will be shipped in large volume by our customers to their customers, however.

Expand Adoption of the GigaChip Interface Protocol

We have provided our GCI interface protocol as an open industry standard that may be designed into other ICs in the system, as we believe this will further enable serial communication on line cards and encourage adoption of our Bandwidth Engine IC products. A number of IC providers and partners have publicly announced their support of GCI and Bandwidth Engine, including the largest FPGA providers -Altera Corporation (a subsidiary of Intel Corporation) and Xilinx, Inc., and EZchip Semiconductor Ltd. (a subsidiary of Mellanox Technologies Ltd.), with whom we work closely to support common customers. In addition, multiple networking systems companies, including actual and prospective customers, have adopted GCI.

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Build Long-Term Relationships with FPGA Vendors and Suppliers of Data Processing Solutions

We believe that having long-term relationships with FPGA providers is critical to our success, as such relationships enable us to reduce our time-to-market, provide us with a competitive advantage and expand our target markets. A key consideration of network system designers is to demonstrate interoperability between our IC products and the processor ICs utilized in their systems. To obtain design wins, we must demonstrate this interoperability, and also show that our IC works optimally with the packet processor to achieve the performance requirements. In addition, our current strategy requires packet processor suppliers to adopt our GCI interface. To that end, we have been working closely with FPGA and application specific standard product providers, to enable interoperability between our Bandwidth Engine IC products and their high-performance products. To facilitate the acceptance of our Bandwidth Engine ICs, we have made available development and characterization kits for system designers to evaluate and develop code for next-generation networking systems. Our characterization kits are fully-functional hardware platforms that allow FPGA and ASIC providers, and their customers, to demonstrate interoperability of the Bandwidth Engine IC with the ASIC or FPGA the designers use within their systems.

Our IC Products

BLAZAR Accelerator Engines

Our Blazar Accelerator Engines, include the Bandwidth Engine, which is targeted for high-performance applications where throughput is critical, and the PHE, which combines the features of the Bandwidth Engine with 32 RISC processors to allow user-defined functions or algorithms to be embedded in the PHE.

Bandwidth Engine

The Bandwidth Engine is a memory-dominated IC that has been designed to be a high-performance companion IC to packet processors. While the Bandwidth Engine primarily functions as a memory device with a high-performance and high-efficiency interface, it also can accelerate certain processing operations by serving as a co-processor element. Our Bandwidth Engine ICs combine: (1) our proprietary high-density, high-speed, low latency embedded memory, (2) our high-speed serial interface technology, or SerDes, (3) an open-standard interface protocol and (4) intelligent access technology. We believe an IC combining our 1T-SRAM memory and serial interface with logic and other intelligence functions provides a system-level solution and significantly improves overall system performance at lower cost, size and power consumption. Our Bandwidth Engine ICs can provide up to and over 6.5 billion memory accesses per second externally and 12 billion memory accesses per second internally, which is more than three times the performance of current memory-based solutions. They also can enable system designers to significantly narrow the gap between processor and memory IC performance. Customers that design Bandwidth Engine ICs onto the line cards in their networking systems will re-architect their systems at the line-card level and use our product to replace traditional memory solutions. When compared with existing commercially available solutions, our Bandwidth Engine ICs may:

- provide up to four times the performance;
- reduce power consumption by approximately 50%;
- reduce cost by greater than 50%; and
- result in a dramatic reduction in IC pin counts on the line card.

Our first-generation Bandwidth Engine IC products contain 576 megabytes, or MB, of memory and use a serial interface with up to 16 lanes operating at up to 10.3 Gbps per lane. We announced the end-of-life of these products and expect to complete fulfillment of last-time customer orders in the first half of 2019.

Our second-generation Bandwidth Engine IC products contain 576 MB of memory and use a SerDes interface with up to 16 lanes operating at up to 12.5 Gbps per lane. In addition to a speed improvement of up to 50% over our first-generation products, the architecture has enabled multiple family-member parts with added specialized features. We have been shipping our Bandwidth Engine 2 IC products since 2013. We continue to win new designs for this device family, and expect these products to be our primary revenue source for the foreseeable future.

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Our third-generation Bandwidth Engine IC products contain 1152 MB of memory and use a SerDes interface with up to 16 lanes operating at up to 25 Gbps per lane. Our Bandwidth Engine 3 ICs target support for packet-processing applications with up to five billion memory single word accesses per second, as well as burst mode to enable full duplex buffering up to 400 Gbps for ingress, egress and oversubscription applications. The devices provide benefits of size, power, pin count and cost savings to our customers. We do not anticipate customer production revenues from these products until the second half of 2019 or later.

Programmable HyperSpeed Engine (PHE)

Our PHE IC products further leverage our proven serial interface technology and high-density integrated memory with the processor engine architecture to enable high-speed customizable search, security, and data analysis functions for networking, security, and data center applications, as well as new markets such as video and compute acceleration. Our PHE architecture features 32 search-optimized processor engines, data flow schedulers, and over a terabit of internal access bandwidth. The device leverages our GCI interface technology and high-density integrated memory (1152 Mb of 1T-SRAM embedded memory).

LineSpeed Flex PHYs

Our LineSpeed Flex family of 100G PHYs, is designed to support industry standards and includes gearbox, Multi-Link Gearbox, or MLG, and high density CDR/retimer devices designed to enable Ethernet and OTN line card applications to support the latest electrical and optical interfaces. To date, we have announced four unique devices in this product family:

- MSH320, a 100Gbps Gearbox with RS-FEC: For adapting 10x10 to 4x25 from 100Gbps optical standards to a host ASIC, MAC/Framer, NPU or FPGA with 10x10G interfaces. The MSH320 includes an integrated Reed-Solomon forward error correction, or RS-FEC, option to enable systems to also support 100G electrical and optical standards. The device also includes a 10x10Gbps retimer to allow seamless support of 10 and 40Gbps interfaces;
- MSH225, a 10 Lane Full-Duplex Retimer: For high-density retiming applications where the line rates may be up to 28Gbps per lane and connect to host ASIC, framer, NPU or FPGA ICs equipped with 25Gbps interfaces. Each one of the 20 total independent lanes can be configured to support 10, 25, 40 or 100Gbps standards. The MSH225 integrates optional 100Gbps RS-FEC capability;
- MSH322, a 100Gbps Multi-Link Gearbox for Line Cards for support of high-density, independent 10GE and 40GE interfaces multiplexed into a 100GE (4x25Gbps) host interface, while supporting electrical and optical industry standards. The device enables line cards with high-density switches based on 25Gbps interfaces to support two times the density of 10 and 40Gbps ports; and
- MSH321, a derivative Multi-Link Gearbox built into a highly compact package and optimized layout to support the MLG function in module and compact daughter card applications.

We are shipping production quantities of our LineSpeed products to a lead customer, and expect to begin generating meaningful recurring revenue from sales to this customer in 2019.

IP Licensing and Distribution

Historically, we have offered our memory and interface technologies on a worldwide basis to semiconductor companies, electronic product manufacturers, foundries, intellectual property companies and design companies through product development, technology licensing and joint marketing relationships. We licensed our IP technology to semiconductor companies who incorporated our technology into ICs that they sold to their customers. As a result of the change in our corporate strategy, since early 2012, our IP licensing activities have been limited, and we expect this to continue. Royalty and other revenue generated from our existing IP agreements represented 9%, 11% and 24% of our total revenue in 2018, 2017 and 2016, respectively. Royalty revenues have been declining since 2010, and we expect them to continue to decline in 2019.

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Research and Development

Our ability to compete in the future depends on successfully improving our technology to meet the market's increasing demand for higher performance and lower cost solutions. Development of our IC products requires specialized chip design and product engineers, as well as significant fabrication and testing costs, including mask costs, as we bring these products to market. During 2017, we substantially reduced our headcount, and currently have limited internal resources available for new IC product development, which will result in fewer product improvements and new developments. In the near term, our planned product roadmap will include software-based capabilities and features that leverage our existing base of IC products.

Sales and Marketing

We believe that systems OEMs typically prefer to extend the use of traditional memory solutions and their parallel interfaces, despite performance and costs challenges, and are reluctant to change their technology platforms and adopt new designs and technologies, such as serial interfaces, which are an integral part of our product solutions. Therefore, our principal selling and marketing activities to date have been focused on persuading these OEMs and key component specialists that our solutions provide critical performance advantages, as well as on securing design wins with them.

In addition to our direct sales personnel, we sell through sales representatives and distributors in the United States and Asia. We also have applications engineers who support our customer engagements and engage with the customers' system architects and designers to propose and implement our IC and IP solutions, such as the GCI interface, to address their systems challenges.

In the markets we serve, the time from a design win to production volume shipments can range from 18 to 36 months. Networking, communications and security appliance systems can have a product life from a few years to over 10 years once a product like ours has been designed into the system.

Our revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2018, Flextronics, which primarily purchases on behalf of Palo Alto Networks, Inc. and Nokia, formerly Alcatel-Lucent, Clavis Company, formerly Kogent, our Japanese IC distributor, Palo Alto Networks and Nokia, represented 32%, 18%, 18% and 15% of total revenue, respectively. For the year ended December 31, 2017, Flextronics, Clavis Company, and Nokia, represented 46%, 17% and 11% of total revenue, respectively. For the year ended December 31, 2016, Alcatel-Lucent, Clavis Company and Taiwan Semiconductor Manufacturing Co., Ltd., or TSMC, represented 47%, 21% and 13% of our total revenue, respectively.

Intellectual Property

We regard our patents, copyrights, trademarks, trade secrets and similar intellectual property as critical to our success, and rely on a combination of patent, trademark, copyright, and trade secret laws to protect our proprietary rights.

As of December 31, 2018, we held 67 U.S. and 42 foreign patents on various aspects of our technology, with expiration dates ranging from 2019 to 2036. We also held 8 pending patent applications in the U.S. and abroad. There can be no assurance that others will not independently develop or patent similar or competing technology or design around any patents that may be issued to us, or that we will be able to successfully enforce our patents against infringement by others.

The semiconductor industry is characterized by frequent litigation regarding patent and other intellectual property rights. Our licensees or we might, from time to time, receive notice of claims that we have infringed patents or other intellectual property rights owned by others. Our successful protection of our patents and other intellectual property rights and our ability to make, use, import, offer to sell, and sell products free from the intellectual property rights of others are subject to a number of factors, particularly those described in Part I, Item 1A, “Risk Factors.”

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Competition

The markets for our products are highly competitive. We believe that the principal competitive factors are:

- processing speed and performance;
- density and cost;
- power consumption;
- reliability;
- interface requirements;
- ease with which technology can be customized for and incorporated into customers' products; and
- level of technical support provided.

We believe that our products compete favorably with respect to each of these criteria. Our proprietary 1T-SRAM embedded memory and high-speed serial interface IP can provide our Bandwidth Engine ICs with a competitive advantage over alternative devices. Alternative solutions are either DRAM or SRAM-based and can support either the memory size or speed requirements of high-performance networking systems, but generally not both. DRAM solutions provide a significant amount of memory at competitive cost, but DRAM solutions do not have the required fast access and cycle times to enable high-performance. The DRAM solutions currently used in networking systems include RLDRAM from Micron Technology, Inc., or Micron, LLDRAM from Renesas, DDR from Samsung Electronics Co., Ltd., Micron and others, and HBM, which is stacked memory from Samsung Electronics Co. and SK Hynix. SRAM solutions can meet high-speed performance requirements, but often lack adequate memory size. The SRAM solutions currently used in networking systems primarily include QDR or similar SRAM products from Cypress Semiconductor Corporation and GSI Technology, Inc. Most of the currently available SRAM and DRAM solutions use a parallel, rather than a serial interface. To offset these drawbacks, system designers generally must use more discrete memory ICs, resulting in higher power consumption and greater utilization of space on the line card.

Our competitors include established semiconductor companies with significantly longer operating histories, greater name recognition and reputation, large customer bases, dedicated manufacturing facilities and greater financial, technical, sales and marketing resources. This may allow them to respond more quickly than us to new or emerging technologies or changes in customer requirements. Generally, customers prefer suppliers with greater financial resources than we have currently. Many of our competitors also have significant influence in the semiconductor industry. They may be able to introduce new technologies or devote greater resources to the development, marketing and sales of their products than we can. Furthermore, in the event of a manufacturing capacity shortage, these competitors may be able to manufacture products when we are unable to do so.

Our Bandwidth Engine and PHE ICs compete with embedded memory solutions, stand-alone memory ICs, including both DRAM and SRAM ICs, ASICs designed by customers in-house to meet their system requirements, and NPUs that use significant internal memory and customer-designed software to implement tasks. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has limited history of manufacturing such ICs and limited financial resources. In addition, Bandwidth Engine and PHE ICs require the customer and its other IC suppliers to implement our chip-to-chip communication protocol, the GCI interface. These parties may be unwilling to do this if they believe it could adversely impact their own future product developments or competitive advantages, or, if they believe it might complicate their development process or increase the cost of their products. To remain competitive, we believe we must provide unparalleled memory IC solutions with the highest bandwidth capability for our target markets, which solutions are engineered and built for high-reliability carrier and enterprise applications.

Our LineSpeed PHY ICs compete with solutions offered by Broadcom Ltd., Inphi Corporation, M/A-COM Technology Solutions Holdings, Inc. and Semtech Corp., as well as other smaller analog signal processing companies. We also may compete with ASICs designed by customers in-house to meet their system requirements, as well as by optical module OEMs. The market for our LineSpeed products is highly competitive, and customers have a number of suppliers they can choose from. We must provide differentiated features with a reasonable IC power budget, while offering competitive pricing.

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Manufacturing

We depend on third-party vendors to manufacture, package, assemble and test our IC products, as we do not own or operate a semiconductor fabrication, packaging or production testing facility for boards and system assembly. By outsourcing manufacturing, we can avoid the high cost associated with owning and operating our own facilities, allowing us to focus our efforts on the design and marketing of our products.

We perform an ongoing review of product manufacturing and testing processes. Our IC products are subjected to extensive testing to assess whether their performance meets design specifications. Our test vendors provide us with immediate test data and the ability to generate characterization reports that are made available to our customers. We have achieved ISO 9001:2015 certification, and all of our significant manufacturing vendors have also achieved ISO 9001 certification.

Employees

As of December 31, 2018, we had 21 employees all of whom are located in the United States, consisting of 13 in research and development and manufacturing operations and 8 in sales, general and administrative functions.

Available Information

We were founded in 1991 and reincorporated in Delaware in September 2000. Our website address is www.mosys.com. The information in our website is not incorporated by reference into this report. Through a link on the Investor section of our website, we make available our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Securities Exchange Act of 1934, as soon as reasonably practicable after they are filed with, or furnished to, the Securities and Exchange Commission, or SEC. You can also read any materials submitted electronically by us to the SEC on its website (www.sec.gov), which contains reports, proxy and information statements, and other information regarding issuers that file electronically with the SEC, including us.

Item 1A. Risk Factors

We have a history of losses and we will need to raise additional capital in the future.

We recorded a net loss of approximately $11.4 million for the year ended December 31, 2018, and ended the period with an accumulated deficit of approximately $236 million. We recorded a net loss of approximately $10.7 million for the year ended December 31, 2017, and ended the period with an accumulated deficit of approximately $225 million. These and prior-year losses have resulted in significant negative cash flows and have required us to raise substantial amounts of additional capital during this period. To remain competitive and expand our product offerings to customers, we will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit and sufficient cash flows to continue doing business without raising additional capital from time to time. Given our history of fluctuating revenues and operating losses, the expected reduction in royalty and licensing revenues and challenges we face in securing customers for our IC products, we cannot be certain that we will be able to achieve and maintain profitability on either a quarterly or annual basis in the future.

Our failure to raise additional capital or generate the significant capital necessary to expand our operations and invest in new products could reduce our ability to compete and could harm our business.

We intend to continue spending to grow our business. Despite the successful completion of our public offering and repayment of a portion of and extension of the repayment date for our Senior Secured Convertible Notes in October 2018, we still might need to obtain additional financing to pursue our business strategy, develop new products, respond to competition and market opportunities and acquire complementary businesses or technologies, in addition to repaying these notes. There can be no assurance that such additional capital, whether in the form of debt or equity financing, will be sufficient or available and, if available, that such capital will be offered on terms and conditions acceptable to us.

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If we were to raise additional capital through sales of our equity securities, our stockholders would suffer dilution of their equity ownership, as exemplified by the substantial share dilution resulting from our October 2018 public offering. If we engage in a subsequent debt financing, we may be required to accept terms that restrict our ability to incur additional indebtedness, prohibit us from paying dividends, repurchasing our stock or making investments, and force us to maintain specified liquidity or other ratios, any of which could harm our business, operating results and financial condition. If we need additional capital and cannot raise it on acceptable terms, we may not be able to, among other things:

- Develop or enhance our products;
- Continue to expand our product development and sales and marketing organizations;
- Acquire complementary technologies, products or businesses;
- Expand operations, in the United States or internationally;
- Hire, train and retain employees; or
- Respond to competitive pressures or unanticipated working capital requirements.

Our failure to do any of these things could seriously harm our ability to execute our business strategy and may force us to curtail our research and development plans or existing operations.

Our success depends upon the acceptance of our integrated circuits, or ICs, by equipment suppliers to the cloud networking, security and other systems markets. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has a limited history of manufacturing such ICs. For example, our Bandwidth Engine and PHE IC products require our customers and their other IC suppliers to implement our proprietary GCI chip-to-chip communication protocol, which they may be unwilling to do. In the past, we have experienced reluctance by potential customers to adopt the GCI interface. Thus, currently, we do not know whether we will be able to generate adequate profit from making and selling our products.

An important part of our strategy to gain market acceptance is to penetrate new markets by targeting market leaders to accept our IC solutions. This strategy is designed to encourage other participants in those markets to follow these leaders in adopting our solutions. If a high-profile industry participant adopts our ICs for one or more of its products but fails to achieve success with those products, or is unable to successfully implement our ICs, other industry participants' perception of our solutions could be harmed. Any such event could reduce the amount of future sales of our IC products.

Future revenue growth depends on our winning designs with existing and new customers, retaining current customers, and having those customers design our solutions into their product offerings and successfully selling and marketing such products. If we do not continue to win designs in the short term, our product revenue in the following years will not grow.

We sell our ICs to OEM customers that include our ICs in their products. Our technology is generally incorporated into products at the design stage, which we refer to as a design win, and which we define as the point at which a customer has made a commitment to build a board against a fixed schematic for its system, and this board will utilize our ICs. As a result, our future revenue depends on our OEM customers designing our ICs into their products, and on those products being produced in volume and successfully commercialized. If we fail to retain our current customers or convince our current or prospective customers to include our ICs in their products and fail to achieve a consistent number of design wins, our results of operations and business will be harmed. In addition, if a current or prospective customer designs a competitor's offering into its product, it becomes significantly more difficult for us to sell our IC solutions to that customer because changing suppliers involves significant cost, time, effort and risk for the OEM.

Even if a customer designs one of our ICs into its product, we cannot be assured that the OEM's product will be commercially successful over time or at all or that we will receive or continue to receive any revenue from that customer. Furthermore, the customer product for which we obtain a design win may be canceled before the product enters production or before or after it is introduced into the market. Because of our extended sales cycle, our revenue in future years is highly dependent on design wins we are awarded today. Our lack of capital and uncertainty about our future technology roadmap also may limit our success in achieving additional design wins, as discussed under, "We may experience difficulties in transitioning to new wafer fabrication process technologies or in achieving higher levels of design integration, which may result in reduced manufacturing yields, delays in product deliveries and increased costs."

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The design-win process is generally a lengthy, expensive and competitive process, with no guarantee of revenue, and, if we fail to generate sufficient revenue to offset our expenses, our business and operating results would suffer.

Achieving a design win is typically a lengthy, expensive and competitive process because our customers generally take a considerable amount of time to evaluate our ICs. In the markets we serve, the time from initial customer engagement to design win to production volume shipments can range from two to three years, though it may take longer for new customers or markets we intend to address. In order to win designs, we are required to both incur design and development costs and dedicate substantial engineering resources in pursuit of a single customer opportunity. Even though we incur these costs, we may not prevail in the competitive selection process, and, even if we do achieve a design win, we may never generate sufficient, or any, revenue to offset our development expenditures. Our customers have the option to decide whether or not to put our solutions into production after initially designing our products in the specification. The customer can make changes to its product after a design win has been awarded to us, which can have the effect of canceling a previous design win. This occurred in 2018 when a large customer decided to phase out its use of our products. The delays inherent in our protracted sales cycle increase the risk that a customer will decide to cancel, curtail, reduce or delay its product plans, causing us to lose anticipated revenue. In addition, any change, delay or cancellation of a customer's plans could harm our financial results, as we may have incurred significant expense while generating no revenue.

If our foundries do not achieve satisfactory yields or quality, our cost of net revenue will increase, our operating margins will decline, and our reputation and customer relationships could be harmed.

We depend not only on sufficient foundry manufacturing capacity and wafer prices, but also on good production yields (the number of good die per wafer) and timely wafer delivery to meet customer demand and maintain profit margins. The fabrication of our products is a complex and technically demanding process. Minor deviations in the manufacturing process can cause substantial decreases in yields, and in some cases, cause production to be suspended. Our foundry, Taiwan Semiconductor Manufacturing Company, or TSMC, from time to time, experiences manufacturing defects and reduced manufacturing yields. Changes in manufacturing processes or the inadvertent use of defective or contaminated materials by our foundries could result in lower than anticipated manufacturing yields, which would harm our revenue or increase our costs. For example, in the past, our foundry produced ICs and met its process specification range but did not meet our customer's specifications causing us to write off a portion of our production lot. Many of these problems are difficult to detect at an early stage of the manufacturing process and may be time consuming and expensive to correct. Poor yields from our foundry, or defects, integration issues or other performance problems in our ICs, could cause us significant customer relations and business reputation problems, harm our operating results and give rise to financial or other damages to our customers. Our customers might consequently seek damages from us for their losses. A product liability claim brought against us, even if unsuccessful, would likely be time consuming and costly to defend.

We may experience difficulties in transitioning to new wafer fabrication process technologies or in achieving higher levels of design integration, which may result in reduced manufacturing yields, delays in product deliveries and increased costs.

We aim to use the most advanced manufacturing process technology appropriate for our solutions that is available from TSMC. As a result, we periodically evaluate the benefits of migrating our solutions to other technologies in order to improve performance and reduce costs. These ongoing efforts require us from time to time to modify the manufacturing processes for our products and to redesign some products, which in turn may result in delays in product deliveries. We are dependent on TSMC to support the production of wafers for future versions of our ICs, as TSMC is our sole foundry. Such production may require changes to TSMC's existing process technology. If TSMC elects to not

alter their process technology to support future versions of our ICs, we would need to identify a new foundry.

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In addition, our 1T-SRAM technology used in our Bandwidth Engine and PHE products is not available at process nodes below 40 nanometers. To date, we have not developed any memory products below the 40-nanometer process node. To continue the product roadmap for our Bandwidth Engine and PHE products, we will need to identify a new foundry and/or no longer use our 1T-SRAM technology. We do not consider this to adversely affect our current product offerings, but we expect to face difficulties, delays and increased expense as we transition our products to new processes, and potentially to new foundries for future products. For example, we believe our next generation of products will need to be designed using a FinFET process, which will require us to incur significantly high development costs for mask tooling and computer-aided design software. We currently lack the funds to pay for such development costs. Moreover, an inability to continue our product roadmap can adversely affect, and has in the past affected our efforts to win new customers, secure additional design wins and significantly grow our future revenues.

Because the manufacturing of integrated circuits is extremely complex, the process of qualifying a new foundry is a lengthy process and there can be no assurance that we will be able to find and qualify replacement suppliers without materially adversely affecting our business, financial condition, results of operations and prospects for future growth. We cannot assure you that we will be able to maintain our relationship with our current foundry or develop relationships with new foundries. If we or TSMC experience significant delays in transitioning to smaller geometries or fail to efficiently implement transitions, we could experience reduced manufacturing yields, delays in product deliveries and increased costs, any of which could harm our relationships with our customers and our operating results.

We may not achieve the anticipated benefits of a fabless semiconductor company by developing and bringing to market our IC products.

Our goal is to increase our total available market by creating high-performance ICs for networking communications and data center systems, using our proprietary technology and design expertise. In recent years, this development effort has required that we add headcount and design resources, such as expensive software tools, which has increased our losses from, and cash used in, operations. Due to our limited financial resources, we have been unable to sustain these development efforts and curtailed them in 2017. We may not be successful in our development efforts to bring our ICs to market successfully nor be successful in selling ICs due to various risks and uncertainties, including, but not limited to:

- a lack of working capital;
- customer acceptance;
- adoption of the GCI interface, without which our Bandwidth Engine and PHE products cannot function;
- difficulties and delays in our product development, manufacturing, testing and marketing activities;
- timeliness of new product introductions;
- the anticipated costs and technological risks of developing and bringing ICs to market;
- the willingness of our manufacturing partners to assist successfully with fabrication;
- our ability to qualify our products for mass production and achieve wafer yield levels and the final test results necessary to be price competitive;
- the availability of quantities of ICs supplied by our manufacturing partners at a competitive cost;
- our ability to generate the desired gross margin percentages and return on our product development investment;
- competition from established IC suppliers;
- the adequacy of our intellectual property protection for our proprietary IC designs and technologies;

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- customer concerns over our financial condition and viability to be a long-term profitable supplier;
- the vigor and growth of markets served by our current and prospective customers; and
- our lack of recent experience as a fabless semiconductor company making and selling proprietary ICs.

If we experience significant delays in bringing our IC products to market or if customer adoption of our products is delayed, this could have a material adverse effect on our anticipated revenues in upcoming years due to the potential loss of design wins and future revenues. We could experience significant delays in the future.

Our main objective is the development and sale of our products to cloud networking, security, test and video system providers and their subsystem and component vendors, and, if demand for these products does not grow, we may not achieve revenue growth and our strategic objectives.

We market and sell our ICs to cloud networking, communications, data center and other equipment providers and their subsystem and component vendors. We believe our future business and financial success depends on market acceptance and increasing sales of these products. In order to meet our growth and strategic objectives, networking infrastructure OEMs must incorporate our products into their systems, and the demand for their systems must grow as well. We cannot provide assurance that sales of our products to these OEMs will increase substantially in the future or that the demand for our customers' systems will increase. Our future revenues from these products may not increase in accordance with our growth and strategic objectives, if, instead, our OEM customers modify their product designs, select products sold by our competitors or develop their own proprietary ICs. Moreover, demand for their products that incorporate our ICs may not grow or result in significant sales of such products due to factors affecting the customers and their business, such as industry downturns, declines in capital spending in the enterprise and carrier markets and unfavorable macroeconomic conditions. Thus, the future success of our business depends in large part on factors outside our control, and sales of our products may not meet our revenue growth and strategic objectives.

Our failure to continue to develop new products and enhance our products on a timely basis could diminish our ability to attract and retain customers.

The existing and potential markets for our products are characterized by ever-increasing performance requirements, evolving industry standards, rapid technological change and product obsolescence. These characteristics lead to periodic changes in customer requirements, shorter product life cycles and changes in industry demands and mandate new product introductions and enhancements to maintain customer engagements and design wins. In order to attain and maintain a significant position in the market, we will need to continue to enhance and evolve our products and the underlying proprietary technologies in anticipation of these market trends, although we do not have a large engineering staff.

Our future performance depends on a number of factors, including our ability to:

- identify target markets and relevant emerging technological trends;
- develop and maintain competitive technology by improving performance and adding innovative features that differentiate our products from alternative technologies;
- enable the incorporation of our products into customers' products on a timely basis and at competitive prices;
- develop our products to be manufactured at smaller process geometries; and
- respond effectively to new technological developments or new product introductions by others.

Our failure to enhance our existing IC products and develop future products that achieve broad market acceptance will harm our competitive position and impede our future growth.

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Our ICs have a lengthy sales cycle, which makes it difficult to predict success in this market and the timing of future revenue.

Our ICs have a lengthy sales cycle, ranging from six to 24 months from the date of our initial proposal to a prospective customer until the date on which the customer confirms that it has designed our product into its system. As lengthy, or an even lengthier period, could ensue before we would know the volume of products that such customer will, or is likely to, order. A number of factors can contribute to the length of the sales cycle, including technical evaluations of our products by the customers, the design process required to integrate our products into the customers' products and the timing of the customers' new product announcements. In anticipation of product orders, we may incur substantial costs before the sales cycle is complete and before we receive any customer payments. As a result, in the event that a sale is not completed or is cancelled or delayed, we may have incurred substantial expenses, making it more difficult for us to become profitable or otherwise negatively impacting our financial results. Furthermore, because of this lengthy sales cycle, the recording of revenues from our selling efforts may be substantially delayed, our ability to forecast our future revenue may be more limited and our revenue may fluctuate significantly from quarter to quarter. We cannot provide any assurances that our efforts to build a strong and profitable business based on the sale of ICs will succeed. If these efforts are not successful, in light of the substantial resources that we have invested, our future operating results and cash flows could be materially and adversely affected.

The semiconductor industry is cyclical in nature and subject to periodic downturns, which can negatively affect our revenue.

The semiconductor industry is cyclical and has experienced pronounced downturns for sustained periods of up to several years. To respond to any downturn, many semiconductor manufacturers and their customers will slow their research and development activities, cancel or delay new product developments, reduce their workforces and inventories and take a cautious approach to acquiring new equipment and technologies. As a result, our business has been in the past and could be adversely affected in the future by an industry downturn, which could negatively impact our future revenue and profitability. Also, the cyclical nature of the semiconductor industry may cause our operating results to fluctuate significantly from year-to-year, which may tend to increase the volatility of the price of our common stock.

We expect our royalty revenues to decrease compared with our historical results, and there is no guarantee revenues from our IC products will replace these lost revenues in the near future.

In 2011, we began to place greater emphasis on our IC business and re-deploy engineering, marketing and sales resources from IP to IC activities. We are no longer actively pursuing new license arrangements, and, as a result, our royalty and other revenues in 2018 declined when compared with prior years. In addition, the production volumes of the current royalty-bearing products shipped by our licensees are expected to decrease; therefore we expect our royalty revenue to decrease in 2019 and future periods. Historically, royalties have generated a 100% gross margin, and any decrease in royalties adversely affects our gross margin, operating results and cash flows.

Our revenue has been highly concentrated among a small number of customers, and our results of operations could be harmed if we lose a key revenue source and fail to replace it.

Our overall revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2018, our three largest customers represented 32%, 18% and 18% of total revenue, respectively. For the year ended December 31, 2017, our three largest customers represented 46%, 17% and 11% of total revenue, respectively. For the year ended December 31, 2016, our three largest customers

represented 47%, 21% and 13% of total revenue, respectively. We expect that a relatively small number of customers will continue to account for a substantial portion of our revenue for the foreseeable future. However, in mid-2018, we were informed by a large customer that it will be phasing out our Bandwidth Engine IC products over the next 18 months. The loss of future business with this customer has adversely impacted our revenue outlook for 2019.

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As a result of this revenue concentration, our results of operations could be adversely affected by the decision of a single key customer to cease using our technology or products or by a decline in the number of products that incorporate our technology that are sold by a single licensee or customer or by a small group of licensees or customers.

Our revenue concentration may also pose credit risks, which could negatively affect our cash flow and financial condition.

We might also face credit risks associated with the concentration of our revenue among a small number of licensees and customers. As of December 31, 2018, three customers represented 63% of total trade receivables. Our failure to collect receivables from any customer that represents a large percentage of receivables on a timely basis, or at all, could adversely affect our cash flow or results of operations and might cause our stock price to fall.

Our products must meet exact specifications, and defects and failures may occur, which may cause customers to return or stop buying our products.

Our customers generally establish demanding specifications for quality, performance and reliability that our products must meet. However, our products are highly complex and may contain defects and failures when they are first introduced or as new versions are released. If defects and failures occur in our products during the design phase or after, we could experience lost revenues, increased costs, including warranty and customer support expenses and penalties for non-performance stipulated in customer purchase agreements, delays in or cancellations or rescheduling of orders or shipments, product returns or discounts, diversion of management resources or damage to our reputation and brand equity, and in some cases consequential damages, any of which would harm our operating results. In addition, delays in our ability to fill product orders as a result of quality control issues may negatively impact our relationship with our customers. We cannot assure you that we will have sufficient resources to satisfy any asserted claims. Furthermore, any such defects, failures or delays may be particularly damaging to us as we attempt to establish our reputation as a reliable provider of IC products.

Because we sell our products on a purchase order basis and rely on estimated forecasts of our customers' needs, inaccurate forecasts could adversely affect our business.

We sell our IC products pursuant to individual purchase orders, rather than long-term purchase commitments. Therefore, we will rely on estimated demand forecasts, based upon input from our customers, to determine how much product to manufacture. Because our sales will be based primarily on purchase orders, our customers may cancel, delay or otherwise modify their purchase commitments with little or no notice to us. For these reasons, we will generally have limited visibility regarding our customers' product needs. In addition, the product design cycle for networking OEMs is lengthy, and it may be difficult for us to accurately anticipate when they will commence commercial shipments of products that include our ICs.

Furthermore, if we experience substantial warranty claims, our customers may cancel existing orders or cease to place future orders. Any cancellation, delay or other modification in our customers' orders could significantly reduce our revenue, cause our operating results to fluctuate from period to period, and make it more difficult for us to predict our revenue. In the event of a cancellation or reduction of an order, we may not have enough time to reduce operating expenses to mitigate the effect of the lost revenue on our business.

If we overestimate customer demand for our products, we may purchase products from our manufacturers that we cannot sell. Conversely, if we underestimate customer demand or if sufficient manufacturing and testing capacity were

unavailable, we would forego revenue opportunities and could lose market share in the markets served by our products and could incur penalty payments under our customer purchase agreements. In addition, our inability to meet customer requirements for our products could lead to delays in product shipments, force customers to identify alternative sources and otherwise adversely affect our ongoing relationships with our customers.

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We depend on contract manufacturers for a significant portion of our revenue from the sale of our IC products.

Many of our current and prospective OEM customers use third party contract manufacturers to manufacture their systems, and these contract manufacturers purchase our products directly from us on behalf of the OEMs. Although we expect to work with our OEM customers in the design and development phases of their systems, these OEMs often give contract manufacturers some authority in product purchasing decisions. If we cannot compete effectively for the business of these contract manufacturers, or, if any of the contract manufacturers that work with our OEM customers experience financial or other difficulties in their businesses, our revenue and our business could be adversely affected. For example, if a contract manufacturer becomes subject to bankruptcy proceedings, we may not be able to obtain our products held by the contract manufacturer or recover payments owed to us by the contract manufacturer for products already delivered to the contract manufacturer. If we are unable to persuade contract manufacturers to purchase our products, or if the contract manufacturers are unable to deliver systems with our products to OEMs on a timely basis, our business would be adversely affected.

We rely on independent foundries and contractors for the manufacture, assembly, testing and packaging of our integrated circuits, and the failure of any of these third parties to deliver products or otherwise perform as requested could damage our relationships with our customers and harm our sales and financial results.

As a fabless semiconductor company, we rely on third parties for substantially all of our manufacturing operations. We depend on these parties to supply us with material in a timely manner that meets our standards for yield, cost and quality. We do not have long-term supply contracts with any of our suppliers or manufacturing service providers, and therefore they are not obligated to manufacture products for us for any specific period, in any specific quantity or at any specified price, except as may be provided in a particular purchase order. Any problems with our manufacturing supply chain could adversely impact our ability to ship our products to our customers on time and in the quantity required, which in turn could damage our customer relationships and impede market acceptance of our IC solutions.

Our third-party wafer foundries, and testing and assembly vendors are located in regions at high risk for earthquakes and other natural disasters. Any disruption to the operations of these foundries and vendors resulting from earthquakes or other natural disasters could cause significant delays in the development, production, shipment and sales of our IC products.

TSMC, which manufactures our products, is located in Asia, as are other foundries we may use in the future. Our vendors that provide substrates and wafer sorting and handle the testing of our products, are headquartered in either Asia or the San Francisco Bay Area of California. Our primary manufacturing operations are located in San Jose, California. The risk of an earthquake in the Pacific Rim region is significant due to the proximity of major earthquake fault lines. The occurrence of earthquakes or other natural disasters could result in the disruption of the wafer foundry or assembly and test capacity of the third parties that supply these services to us and may impede our research and development efforts, as well as our ability to market and sell our products. We may not be able to obtain alternate capacity on favorable terms, if at all.

Any claim that our products or technology infringe third party intellectual property rights could increase our costs of operation and distract management and could result in expensive settlement costs or the discontinuance of our technology licensing or product offerings. In addition, we may incur substantial litigation expense, which would adversely affect our profitability.

The semiconductor industry is characterized by vigorous protection and pursuit of intellectual property rights or positions, which has resulted in often protracted and expensive litigation. We are not aware of any third party

intellectual property that our products or technology would infringe. However, like many companies of our size with limited resources, we have not searched for all potentially applicable intellectual property in the public databases. It is possible that a third party now has, or may in the future obtain, patents or other intellectual property rights that our products or technology may now, or in the future, infringe. Our licensees and IC customers, or we, might, from time to time, receive notice of claims that we have infringed patents or other intellectual property rights of others. Litigation against us can result in significant expense and divert the efforts of our technical and management personnel, whether or not the litigation has merit or results in a determination adverse to us.

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The discovery of defects in our technology and products could expose us to liability for damages.

The discovery of a defect in our technologies and products could lead our customers to seek damages from us. Many of our agreements with customers include provisions waiving implied warranties regarding our technology and products and limiting our liability to our customers. We cannot be certain, however, that the waivers or limitations of liability contained in our agreements with customers will be enforceable.

Royalty amounts owed to us might be difficult to verify, and we might find it difficult, expensive and time-consuming to enforce our license agreements.

The standard terms of our 1T-SRAM license agreements require our licensees to document the manufacture and sale of products that incorporate our technology and generally report this data to us after the end of each quarter. We have the right to audit these royalty reports periodically, although we have not conducted any such audits recently. These audits can be expensive, time-consuming and potentially detrimental to our business relationships. A failure to fully enforce the royalty provisions of our license agreements could cause our revenue to decrease and impede our ability to achieve and maintain profitability.

We might not be able to protect and enforce our intellectual property rights, which could impair our ability to compete and reduce the value of our technology.

Our technology is complex and is intended for use in complex ICs and networking systems. Our licensees' products utilize our embedded memory and/or interface technology, and a large number of companies manufacture and market these products. Because of these factors, policing the unauthorized use of our intellectual property is difficult and expensive. We cannot be certain that we will be able to detect unauthorized use of our technology or prevent other parties from designing and marketing unauthorized products based on our technology. In the event we identify any past or present infringement of our patents, copyrights or trademarks, or any violation of our trade secrets, confidentiality procedures or licensing agreements, we cannot assure you that the steps taken by us to protect our proprietary information will be adequate to prevent misappropriation of our technology. Our inability to adequately protect our intellectual property would reduce significantly the barriers of entry for directly competing technologies and could reduce the value of our technology. Furthermore, we might initiate claims or litigation against third parties for infringement of our proprietary rights or to establish the validity of our proprietary rights. Litigation by us could result in significant expense and divert the efforts of our technical and management personnel, whether or not such litigation results in a determination favorable to us.

Our existing patents might not provide us with sufficient protection of our intellectual property, and our patent applications might not result in the issuance of patents, either of which could reduce the value of our core technology and harm our business.

We rely on a combination of patents, trademarks, trade secret laws and confidentiality procedures to protect our intellectual property rights. We cannot be sure that any patents will be issued from any of our pending applications or that any claims allowed from pending applications will be of sufficient scope or strength, or issued in all countries where our products can be sold, to provide meaningful protection or any commercial advantage to us. Failure of our patents or patent applications to provide meaningful protection might allow others to utilize our technology without any compensation to us.

If we fail to retain key personnel, our business and growth could be negatively affected.

Our business has been dependent to a significant degree upon the services of a small number of executive officers and technical employees. The loss of key personnel could negatively impact our technology development efforts, our ability to deliver products under our existing agreements, maintain strategic relationships with our partners, and obtain new customers. We generally have not entered into employment or non-competition agreements with any of our employees and do not maintain key-man life insurance on the lives of any of our key personnel.

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We may incur additional debt in the future, subject to certain limitations contained in our Senior Secured Convertible Notes.

The degree to which we are leveraged and the restrictions governing our indebtedness could have important consequences including, but not limited to:

- limiting our ability to service all of our debt obligations;
- impacting our ability to incur additional indebtedness or obtain additional financing in the future for working capital, capital expenditures, acquisitions or general corporate or other purposes;
- increasing our vulnerability to general economic downturns and adverse industry conditions;
- limiting our flexibility in planning for, or reacting to, changes in our business and our industry; and
- limiting our ability to engage in certain transactions or capitalize on acquisition or other business opportunities.

If we are in violation of the terms of our Senior Secured Convertible Notes in the future and do not receive a waiver, the note holders could choose to accelerate payment on all outstanding loan balances. If we needed to obtain replacement financing, we may not be able to quickly obtain equivalent or suitable replacement financing. If we are unable to secure alternative sources of funding, such acceleration would have a material adverse impact on our financial condition.

Provisions of our certificate of incorporation and bylaws or Delaware law might delay or prevent a change-of-control transaction and depress the market price of our stock.

Various provisions of our certificate of incorporation and bylaws might have the effect of making it more difficult for a third party to acquire, or discouraging a third party from attempting to acquire, control of our company. These provisions could limit the price that certain investors might be willing to pay in the future for shares of our common stock. Certain of these provisions eliminate cumulative voting in the election of directors, limit the right of stockholders to call special meetings and establish specific procedures for director nominations by stockholders and the submission of other proposals for consideration at stockholder meetings.

We are also subject to provisions of Delaware law that could delay or make more difficult a merger, tender offer or proxy contest involving our company. In particular, Section 203 of the Delaware General Corporation Law prohibits a Delaware corporation from engaging in any business combination with any interested stockholder for a period of three years unless specific conditions are met. Any of these provisions could have the effect of delaying, deferring or preventing a change in control, including without limitation, discouraging a proxy contest or making more difficult the acquisition of a substantial block of our common stock.

Under our certificate of incorporation, our board of directors may issue up to 20,000,000 shares of preferred stock without stockholder approval on such terms as the board might determine. The rights of the holders of common stock will be subject to, and might be adversely affected by, the rights of the holders of any preferred stock that might be issued in the future.

Our stockholder rights plan could prevent stockholders from receiving a premium over the market price for their shares from a potential acquirer.

We adopted a stockholder rights plan that generally entitles our stockholders to rights to acquire additional shares of our common stock when a third party acquires 15% of our common stock or commences or announces its intent to commence a tender offer for at least 15% of our common stock. The plan also includes an exception to permit the acquisition of shares representing more than 15% of our common stock by a brokerage firm that manages independent

customer accounts and generally does not have any discretionary voting power with respect to such shares. This plan could delay, deter or prevent an investor from acquiring us in a transaction that could otherwise result in stockholders receiving a premium over the market price for their shares of common stock. Our intention is to maintain and enforce the terms of this plan, which could delay, deter or prevent an investor from acquiring us in a transaction that could otherwise result in stockholders receiving a premium over the market price for their shares of common stock.

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Potential volatility of the price of our common stock could negatively affect your investment.

We cannot assure you that there will continue to be an active trading market for our common stock. Historically, the stock market, as well as our common stock, has experienced significant price and volume fluctuations. Market prices of securities of technology companies have been highly volatile and frequently reach levels that bear no relationship to the operating performance of such companies. These market prices generally are not sustainable and are subject to wide variations. If our common stock trades to unsustainably high levels, it is likely that the market price of our common stock will thereafter experience a material decline.

In the past, securities class action litigation has often been brought against a company following periods of volatility in the market price of its securities. We could be the target of similar litigation in the future. Securities litigation could cause us to incur substantial costs, divert management's attention and resources, harm our reputation in the industry and the securities markets and negatively impact our operating results.

We are a "smaller reporting company" and, as a result of the reduced disclosure and governance requirements applicable to smaller reporting companies, our common stock may be less attractive to investors.

We are a "smaller reporting company," and we are subject to lesser disclosure obligations in our SEC filings compared to other issuers. Specifically, "smaller reporting companies" are able to provide simplified executive compensation disclosures in their filings, are exempt from the provisions of Section 404(b) of the Sarbanes-Oxley Act requiring that independent registered public accounting firms provide an attestation report on the effectiveness of internal control over financial reporting and have certain other decreased disclosure obligations in their SEC filings, including, among other things, only being required to provide two years of audited financial statements in annual reports. Decreased disclosures in our SEC filings due to our status as a "smaller reporting company" may make it harder for investors to analyze our operating results and financial prospects.

If we fail to maintain compliance with the continued listing requirements of the Nasdaq Capital Market, our common stock may be delisted and the price of our common stock and our ability to access the capital markets could be negatively impacted.

Our common stock currently trades on the Nasdaq Capital Market under the symbol "MOSY." This market has continued listing standards that we must comply with in order to maintain the listing of our common stock. The continued listing standards include, among others, a minimum bid price requirement of $1.00 per share and any of: (i) a minimum stockholders' equity of $2.5 million; (ii) a market value of listed securities of at least $35.0 million; or (iii) net income from continuing operations of $500,000 in the most recently completed fiscal year or in the two of the last three fiscal years. Our results of operations and fluctuating stock price directly impact our ability to satisfy these continued listing standards. In the event we are unable to maintain these continued listing standards, our common stock may be subject to delisting from the Nasdaq Capital Market.

On September 21, 2018, we received a deficiency notification letter from the staff of Nasdaq stating that the bid price for our common stock must close at $1.00 per share or more for a minimum of ten consecutive trading days during the 180 calendar day period ending March 20, 2019 or we might be delisted. As mentioned above, the price of our common stock can be volatile, and there can be no assurance that we will be able to meet the minimum $1.00 bid price requirement or the other NASDAQ continued listing requirements in the future, and we may be subject to delisting as a result. In December 2018, at the 2018 Annual Meeting of Stockholders (the Annual Meeting), our stockholders provided our board of directors with the authority to effect a reverse stock split of our common stock at a ratio determined by the board of directors within a specified range, without reducing the authorized number of shares

of our common stock, to be effected in the sole discretion of the board of directors at any time within one year of the date of the Annual Meeting without further approval or authorization of our stockholders.

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If we are delisted, we would expect our common stock to be traded in the over-the-counter market, which could adversely affect the liquidity of our common stock. Additionally, we could face significant material adverse consequences, including:

- a limited availability of market quotations for our common stock;
- a reduced amount of analyst coverage;
- a decreased ability to issue additional securities or obtain additional financing in the future;
- reduced liquidity for our stockholders;
- potential loss of confidence by customers, collaboration partners and employees; and
- loss of institutional investor interest.

Item 1B. Unresolved Staff Comments

None.

Item 2. Properties

Our principal administrative, sales, marketing, support and research and development functions are located in a leased facility in San Jose, California. We currently occupy approximately 10,000 square feet of space in the San Jose facility, and the lease extends through November 2020. We believe that our existing facility is adequate to meet our current needs.

Item 3. Legal Proceedings

The information set forth under the “Legal Matters” subheading in Note 9 (Commitments and Contingencies) of the Notes to Consolidated Financial Statements in Part II, Item 15, of this Annual Report on Form 10-K is incorporated herein by reference.

Item 4. Mine Safety Disclosures

Not applicable.

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Part II

Item 5. Market for Registrant's Common Equity, Related Stockholder Matters and Issuer Purchases of Equity Securities

Our common stock is currently listed on the Capital Market of the NASDAQ Stock Market under the symbol MOSY.

Holders of Record

As of December 31, 2018, there were five holders of record of our common stock. The actual number of stockholders is greater than this number of record stockholders and includes stockholders who are beneficial owners but whose shares are held in street name by brokers and other nominees. This number of stockholders of record also does not include stockholders whose shares may be held in trust by other entities.

Securities Authorized for Issuance under Equity Compensation Plan

For information regarding securities authorized for issuance under equity compensation plans, please refer to Item 12—Security Ownership of Certain Beneficial Owners and Management and Related Stockholder Matters.

Item 6. Selected Financial Data

Not applicable.

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Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations

This Management's Discussion and Analysis of Financial Condition and Results of Operations should be read in conjunction with the accompanying consolidated financial statements and notes included in this report.

Overview

Our strategy and primary business objective is to be a profitable IP-rich fabless semiconductor company offering ICs that deliver unparalleled memory bandwidth and access rate performance for high-performance data processing in cloud networking, communications, security appliances, video, test and monitoring, and data center systems. Our solutions deliver time-to-market, performance, power, area and economic benefits for system original equipment manufacturers, or OEMs. Our principal product line and source of substantially all of our revenue is the Bandwidth Engine® product family. Bandwidth Engine ICs combine our proprietary 1T-SRAM® high-density embedded memory, integrated macro functions and high-speed serial interface, or SerDes I/O, with our intelligent access technology and a highly efficient interface protocol. Our second-generation Bandwidth Engine, or Bandwidth Engine 2, products are expected to be our primary revenue source through at least 2020, and we expect these products to continue to generate significant revenue thereafter. We expect our third generation Bandwidth Engine, or Bandwidth Engine 3, products and PHE products to commence production and begin generating meaningful revenue in the second half of 2019. Despite our limited new product development efforts, we believe our current product portfolio positions us for future growth and profitability. We will continue to seek third-party funding for new product development efforts.

We incurred net losses of approximately $11 million for each of the years ended December 31, 2018 and 2017 and had an accumulated deficit of approximately $236 million as of December 31, 2018. These and prior year losses have resulted in significant negative cash flows for almost a decade and have necessitated that we raise substantial amounts of additional capital during this period. To date, we have primarily financed our operations through multiple offerings of common stock to investors and affiliates, as well as asset sale transactions and one offering of convertible notes.

We may continue to incur operating losses and will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit and sufficient cash flows to continue doing business without raising additional capital from time to time.

Accounting Change

On January 1, 2018, we adopted Financial Accounting Standards Board (FASB) Accounting Standards Codification Topic 606, Revenue from Contracts with Customers (ASC 606), using the modified retrospective (cumulative effect) transition method. Under this transition method, results for reporting periods beginning January 1, 2018 or later are presented under ASC 606, while prior period results continue to be reported in accordance with previous guidance. The cumulative effect of the initial application of ASC 606 was recognized as an adjustment to accumulated deficit of $0.2 million as of January 1, 2018. Overall, the adoption of ASC 606 did not have a material impact on the consolidated balance sheet as of December 31, 2018, and statement of operations and comprehensive loss and statement of cash flows for the year ended December 31, 2018. ASC 606 also requires additional disclosures about the nature, amount, timing and uncertainty of revenue and cash flows arising from customer contracts, including

significant judgments and changes in judgments and assets recognized from costs incurred to fulfill a contract. As described below, the analysis of contracts under ASC 606 supports the recognition of revenue at a point in time, resulting in revenue recognition timing that is materially consistent with our historical practice of recognizing product revenue when title and risk of loss pass to the customer.

The following table summarizes the impact of the adoption of ASC 606 on revenue, operating expenses and net loss for the year ended December 31, 2018 (in millions):

	As Reported	Adjustments	Amounts without the Adoption of ASC 606
Revenue	$ 16,600	$ 10	$ 16,610
Operating Expenses	$ 21,080	$ —	$ 21,080
Net Loss	$ (11,409)	$ 10	$ (11,399)

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Sources of Revenue

Product. Product revenue is generally recognized at the time of shipment to our customers. An estimated allowance may be recorded, at the time of shipment, for future returns and other charges against revenue consistent with the terms of sale.

Royalty and other. Our licensing contracts typically provide for royalties based on the licensee's use of our memory technology in their currently shipping commercial products. With the adoption of ASC 606 in January 2018, we estimate royalty revenue in the period in which the licensee uses the licensed technology. Payments are received in the following period.

Critical Accounting Policies and Use of Estimates

Our consolidated financial statements are prepared in conformity with accounting principles generally accepted in the United States of America. Note 1 to the consolidated financial statements in Item 15 of this report describes the significant accounting policies and methods used in the preparation of our consolidated financial statements.

We have identified the accounting policies below as some of the more critical to our business and the understanding of our results of operations. These policies may involve estimates and judgments that affect the reported amounts of assets, liabilities, revenues and expenses. Although we believe our judgments and estimates are appropriate, actual future results may differ from our estimates, and if different assumptions or conditions were to prevail, the results could be materially different from our reported results.

Fair Value Measurements of Financial Instruments

We measure the fair value of financial instruments using a fair value hierarchy that prioritizes the inputs to valuation techniques used to measure fair value into three broad levels, as follows:

Level 1—Inputs used to measure fair value are unadjusted quoted prices that are available in active markets for the identical assets or liabilities as of the reporting date.

Level 2—Pricing is provided by third party sources of market information obtained from investment advisors rather than models. We do not adjust for or apply any additional assumptions or estimates to the pricing information we receive from advisors. Our Level 2 securities include cash equivalents and available-for-sale securities, which consisted primarily of corporate debt, and government agency and municipal debt securities from issuers with high quality credit ratings. Our investment advisors obtain pricing data from independent sources, such as Standard & Poor's, Bloomberg and Interactive Data Corporation, and rely on comparable pricing of other securities because the Level 2 securities we hold are not actively traded and have fewer observable transactions. We consider this the most reliable information available for the valuation of the securities.

Level 3—Unobservable inputs that are supported by little or no market activity and reflect the use of significant management judgment are used to measure fair value. These values are generally determined using pricing models for which the assumptions utilize management's estimates of market participant assumptions. The determination of fair value for Level 3 investments and other financial instruments involves the most management judgment and subjectivity.

Valuation of long-lived Assets

We evaluate our long-lived assets for impairment at least annually, or more frequently when a triggering event is deemed to have occurred. This assessment is subjective in nature and requires significant management judgment to forecast future operating results, projected cash flows and current period market capitalization levels. If our estimates and assumptions change in the future, it could result in a material write-down of long-lived assets. We amortize our finite-lived intangible assets, such as developed technology and patent license, on a straight-line basis over their estimated useful lives of three to seven years. We recognize an impairment charge as the difference between the net book value of such assets and the fair value of the assets on the measurement date.

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Goodwill

We determine the amount of potential goodwill impairment by comparing the fair value of the reporting unit with its carrying amount. To the extent the carrying value of a reporting unit exceeds its fair value, a goodwill impairment charge is recognized. We have determined that we have a single reporting unit for purposes of performing our goodwill impairment test. As we use the market approach to determine the step one fair value, the price of our common stock is an important component of the fair value calculation. We review goodwill for impairment on an annual basis or whenever events or changes in circumstances indicate the carrying value of an asset may not be recoverable. We first assess qualitative factors to determine whether it is more-likely-than-not that the fair value of the reporting unit is less than the carrying amount as a basis for determining whether it is necessary to perform an impairment test. We performed our annual test for goodwill impairment as of September 1, 2018, and, due to a decrease in the price per share of our common stock, the test results indicated the goodwill carrying value was greater than its implied fair value. Further, the Company concluded a triggering event had occurred due to the sustained decrease in the price per share of its common stock and related reduced market capitalization as of September 30, 2018 and performed an additional test for impairment of its goodwill asset resulting in further indication that the goodwill carrying value was still greater than its implied fair value. As a result of both of these tests, the Company recorded non-cash impairment charges of $3.2 million during the third quarter of 2018. Further, the Company concluded a triggering event had occurred due to the sustained decrease in the price per share of its common stock and related reduced market capitalization as of December 31, 2018 and performed an additional test for impairment of its goodwill asset resulting in further indication that the goodwill carrying value was still greater than its implied fair value. As a result of this test, the Company recorded non-cash impairment charges of $9.7 million during the fourth quarter of 2018.

Deferred tax valuation allowance

When we prepare our consolidated financial statements, we estimate our income tax liability for each of the various jurisdictions where we conduct business. This requires us to estimate our actual current tax exposure and to assess temporary differences that result from differing treatment of certain items for tax and accounting purposes. These differences result in deferred tax assets, which we show on our consolidated balance sheet under the category of other assets. The net deferred tax assets are reduced by a valuation allowance if, based upon weighted available evidence, it is more likely than not that some or all of the deferred tax assets will not be realized. We must make significant judgments to determine our provision for income taxes, our deferred tax assets and liabilities and any valuation allowance to be recorded against our net deferred tax asset. We believe that utilization of our net operating loss and tax credit carryforwards, which comprise the majority of our deferred tax assets, may be subject to a substantial annual limitation due to the ownership change limitations provided by the Internal Revenue Code and similar state provisions. See Note 4 to the consolidated financial statements in Item 15 of this report for an additional description of these limitations.

Stock-based compensation

We recognize stock-based compensation for equity awards on a straight-line basis over the requisite service period, usually the vesting period, based on the grant-date fair value. We estimate the value of employee stock options on the date of grant using the Black-Scholes model. The determination of fair value of share-based payment awards on the date of grant using an option-pricing model is affected by our stock price, as well as assumptions regarding a number of highly complex and subjective variables. These variables include, but are not limited to, the expected stock price volatility over the term of the awards, and actual and projected employee stock option exercise behaviors. The expected term of options granted is derived from historical data on employee exercises and post-vesting employment

termination behavior. The expected volatility is based on the historical volatility of our stock price.

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Results of Operations

Net Revenue

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
Product	$15,053	$7,833	$4,604	$7,220	92%	$3,229	70%
Percentage of total net revenue	91%	89%	76%				

Product revenue increased in 2018 and 2017 due to increased volume of shipments for our ICs, mainly Bandwidth Engine products, as additional customer design wins commenced production. We expect our product revenues to decrease in 2019, due to the end of life of our Bandwidth Engine 1 product as well as the loss of one of our large Bandwidth Engine 2 IC customers.

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
Royalty and other	$1,547	$1,009	$1,420	$538	53%	$(411)	(29)%
Percentage of total net revenue	9%	11%	24%				

Royalty and other revenue primarily comprises revenue generated from licensing agreements. The increase from 2017 to 2018 was primarily due to a one-time license and service agreement entered into in 2017 for our analog technology, partially offset by a decline in royalty revenue. The decrease from 2016 to 2017 was primarily due to reduced royalties due to a decrease in shipment volumes by licensees whose products incorporate our licensed IP. We expect royalty and other revenue to decline in 2019, as we expect a decline in shipments of units incorporating our technology by licensees, as their products approach their end of life.

Cost of Net Revenue and Gross Profit

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
Cost of net revenue	$6,346	$4,694	$3,075	$1,652	35%	$1,619	53%
Percentage of total net revenue	38%	53%	51%				

	Years Ended December 31,			Year-Over-Year Change	
	2018	2017	2016	2017 to 2018	2016 to 2017

	(dollar amounts in thousands)						
Gross profit	$10,254	$4,148	$2,949	$6,106	147%	$1,199	41%
Percentage of total net revenue	62 %	47 %	49 %				

In each of 2018, 2017 and 2016, cost of net revenue primarily consisted of direct and indirect costs related to the sale of IC products.

Cost of net revenue increased in 2018 and 2017, primarily due to the increase in material and production costs related to our increased IC shipments, as well as inventory write-downs recorded in 2017. We expect the total cost of net revenue to remain consistent as a percentage of total net revenue in the future.

Gross profit increased from 2017 to 2018, primarily due to the increase in IC shipments and improved manufacturing efficiencies and reduced material purchase prices, as well as the increase in royalty and other revenues which generally has little to no associated cost. Gross profit increased from 2016 to 2017, primarily due to the increase in IC shipments, partially offset by the decrease in our royalty and other revenue, which generally has no associated costs.

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Research and Development

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
Research and development	$4,129	$8,158	$18,086	$(4,029)	(49)%	$(9,928)	(55)%
Percentage of total net revenue	25 %	92 %	300 %				

Our research and development expenses include costs related to the development of our IC products and amortization of intangible assets. We expense research and development costs as they are incurred.

The decrease in 2018 compared with 2017 was primarily due to our restructuring activities in 2017 that resulted in a significant decrease in headcount and related salaries and expenses and lower computer-aided software license fees, backend, depreciation and equipment rental charges.

The decrease in 2017 compared with 2016 was primarily due to our restructuring activities in 2017 and 2016 that resulted in a significant decrease in headcount and related salaries and expenses, and non-recurring mask tooling costs for our IC products incurred in 2016, a decrease in computer-aided software license fees, and a decrease in stock-based compensation charges.

Research and development expenses included stock-based compensation expenses of $0.3 million, $0.4 million and $1.6 million for the years ended December 31, 2018, 2017 and 2016, respectively. We expect that total research and development expenses will increase slightly in 2019 as we invest in developing new derivatives of our existing products and complete production qualification of our Bandwidth Engine 3 products.

Selling, General and Administrative (SG&A)

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
SG&A	$4,095	$4,702	$5,693	$(607)	(13)%	$(991)	(17)%
Percentage of total net revenue	25 %	53 %	95 %				

Selling, general and administrative expenses consist primarily of personnel and related overhead costs for sales, marketing, finance, human resources and general management.

Selling, general and administrative expenses decreased for 2018, compared with the prior year, primarily as a result of our 2017 restructuring activities, which resulted in a decrease in related salaries and expenses, as well as a decrease in franchise taxes.

Selling, general and administrative expenses decreased for 2017, compared with the prior year, primarily as a result of our restructuring activities, which resulted in a decrease in headcount and related salaries and expenses and stock-based compensation charges.

Selling, general and administrative expenses included stock-based compensation expense of $0.3 million, $0.3 million and $0.6 million for the years ended December 31, 2018, 2017 and 2016, respectively. We expect total selling, general and administrative expenses to increase slightly in 2019 due to increased marketing efforts.

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Impairment of Goodwill

	Years Ended December 31,			Year-Over-Year Change	
	2018	2017	2016	2017 to 2018	2016 to 2017
	(dollar amounts in thousands)				
Impairment of goodwill	$12,856	$ —	$9,858	$12,856	$ (9,858)
Percentage of total net revenue	77 %	0 %	164 %		

In 2018 and 2016, we recorded goodwill impairment charges. See Note 1 of the consolidated financial statements in Item 15 of this Report for additional disclosure.

Restructuring Charges

	Years Ended December 31,			Year-Over-Year Change	
	2018	2017	2016	2017 to 2018	2016 to 2017
	(dollar amounts in thousands)				
Restructuring charges	$—	$1,321	$676	$ (1,321)	$ 645
Percentage of total net revenue	0%	15 %	11 %		

In 2017, we recorded restructuring charges attributable to a reduction in our workforce and associated operating expenses and facility relocation costs and contractual obligations under computer-aided software design licenses. In 2016, we recorded restructuring charges attributable to a reduction-in-force in the United States and the closure of our operations at our Indian subsidiary. See Note 10 in the consolidated financial statements in Item 15 of this Report for additional disclosure.

Interest expense

	Years Ended December 31,			Year-Over-Year Change			
	2018	2017	2016	2017 to 2018		2016 to 2017	
	(dollar amounts in thousands)						
Interest expense	$582	$927	$687	$(345)	(37)%	$ 240	35 %
Percentage of total net revenue	4 %	10 %	11 %				

Interest expense is incurred on our senior secured convertible notes. We have paid all accumulated interest since issuance of the convertible notes in March 2016 in-kind through the issuance of new senior-secured convertible notes subject to the same terms and conditions. See Note 11 in the consolidated financial statements in Item 15 of this Report for additional disclosure.

Liquidity and Capital Resources

As of December 31, 2018, we had cash and cash equivalents totaling $7.1 million compared with cash and cash equivalents of $3.9 million as of December 31, 2017.

In 2018, we generated $0.3 million in cash from operating activities, which primarily resulted from the net loss of $11.4 million, adjusted for non-cash charges and gains, which included goodwill impairment of $12.9 million, stock-based compensation expenses of $0.7 million, depreciation and amortization expenses of $0.7 million, accrued interest of $0.6 million, and changes to operating assets and liabilities of $3.1 million. The changes in assets and liabilities primarily related to the timing of the collection of receivables from customers and payments to vendors, including purchases of and increases in inventory.

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In 2017, we used $7.6 million in operating activities, which primarily resulted from the net loss of $10.7 million, adjusted for non-cash charges and gains, which included stock-based compensation expenses of $0.7 million, depreciation and amortization expenses of $0.9 million, accrued interest of $0.9 million, and changes to operating assets and liabilities of $0.6 million. The changes in assets and liabilities primarily related to the timing of the collection of receivables from customers and payments to vendors, including purchases of and increases in inventory.

In 2016, we used $17.9 million in operating activities, which primarily resulted from the net loss of $32.0 million, adjusted for non-cash charges and gains, which included impairment of goodwill of $9.9 million, stock-based compensation expenses of $2.2 million, depreciation and amortization expenses of $1.1 million, accrued interest of $0.7 million, and changes to operating assets and liabilities of $0.3 million. The changes in assets and liabilities primarily related to the timing of the collection of receivables from customers, including customer prepayments, and payments to vendors, including purchases of and increases in inventory.

Our investing activities in 2018, 2017 and 2016 consisted of $0.1 million, $0.3 million and $0.6 million, respectively, expended for purchases of fixed assets. The majority of the remaining investing activities for each of 2017 and 2016 consisted of investing our cash in marketable securities, which did not affect our liquidity.

Our financing activities in 2018 primarily consisted of $10.4 million in net proceeds received from the sale of common stock and warrants to purchase common stock in an equity offering completed in October 2018, which were used to repay $7.4 million of our convertible debt. Our financing activities in 2017 primarily consisted of $2.0 million in net proceeds received from the sale of common stock and warrants to purchase common stock in an equity offering completed in July 2017. Our financing activities in 2016 primarily consisted of $7.9 million in net proceeds received from the issuance of the Notes and $0.4 million in proceeds from purchases of common stock under our employee stock purchase plan.

Our future liquidity and capital requirements are expected to vary from quarter to quarter, depending on numerous factors, including:

- level of revenue;
- cost, timing and success of technology development efforts;
- inventory levels, timing of product shipments and length of billing and collection cycles;
- variations in manufacturing yields, materials costs and other manufacturing risks;
- costs of acquiring other businesses and integrating the acquired operations;
- profitability of our business; and
- whether interest payments on the Notes are paid in cash or, at our election, in kind through the issuance of new Notes with identical terms for the accrued interest.

Working Capital

Our primary need for liquidity is to fund working capital requirements of our businesses, capital expenditures and for general corporate purposes. We expect our cash expenditures to exceed receipts in 2019, as our revenues will not be sufficient to offset our working capital requirements. We incurred net losses of approximately $11 million for each of the years ended December 31, 2018 and 2017 and had an accumulated deficit of approximately $236 million as of December 31, 2018. These and prior year losses have resulted in significant negative cash flows for more than a decade and have required us to raise substantial amounts of additional capital during this period. To date, we have primarily financed our operations through multiple offerings of common stock to investors and affiliates, as well as asset sale transactions. In March 2016, we entered into a 10% Senior Secured Convertible Note Purchase Agreement with the purchasers of $8.0 million principal amount of 10% Senior Secured Convertible Notes due August 15, 2018

(the Notes), at par, in a private placement transaction. Accrued interest was payable semi-annually in cash or in-kind through the issuance of identical new Notes, or with a combination of the two, at the Company's option. Through February 15, 2019, the Company had made the interest payments in-kind through the issuance of additional notes totaling approximately $2.1 million. As of December 31, 2018, the outstanding balance of the Notes approximated $2.7 million.

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Additionally, pursuant to amendments to the Notes and related loan documents effective February 2018 and October 2018, the interest rate was reduced to 8%, the maturity date of the Notes has been extended to August 15, 2023, the optional conversion price has been reduced from $8.50 of Note principal per share of common stock to $0.5717 of Note principal per share of common stock, and the redemption purchase price in the event of certain transactions, such as an acquisition, has been reduced from 120% to 100% of the total amount of debt to be redeemed. The Notes restrict our ability to incur any indebtedness for borrowed money, unless such indebtedness by its terms is expressly subordinated to the Notes in right of payment and to the security interest of the Note holder(s) in respect to the priority and enforcement of any security interest in our property securing such new debt; provided that the Note holder(s) security interest and cash payment rights under the Notes shall be subordinate to a maximum of $5 million of indebtedness for a secured accounts receivable line of credit facility under certain conditions. (See Note 11 to the consolidated financial statements included in Item 15 of this Report.)

We expect to raise additional capital, but there can be no assurance that such funding will be available to us on favorable terms, if at all. The failure to raise capital when needed could have a material adverse effect on our business and financial condition. We may not be able to obtain additional financing as needed on acceptable terms, or at all, which may require us to reduce our operating costs and other expenditures, including reductions of personnel, salaries and capital expenditures. Alternatively, or in addition to such potential measures, we may elect to implement additional cost reduction actions as we may determine are necessary and in our best interests. Any such actions undertaken might limit our opportunities to realize plans for revenue growth and we might not be able to reduce our costs in amounts sufficient to achieve break-even or profitable operations.

If we were to raise additional capital through sales of our equity securities, our stockholders would suffer dilution of their equity ownership. If we engage in debt financing, we may be required to accept terms that restrict our ability to incur additional indebtedness, prohibit us from paying dividends, repurchasing our stock or making investments, and force us to maintain specified liquidity or other ratios, any of which could harm our business, operating results and financial condition. If we need additional capital and cannot raise it on acceptable terms, we may not be able to, among other things:

- develop or enhance our products;
- expand our product development and sales and marketing organizations;
- acquire complementary technologies, products or businesses;
- expand operations, in the United States or internationally;
- hire, train and retain employees; or
- respond to competitive pressures or unanticipated working capital requirements.

Our failure to do any of these things could seriously harm our ability to execute our business strategy and may force us to curtail our research and development plans or existing operations.

Off-Balance Sheet Arrangements

We do not maintain any off-balance sheet arrangements or obligations that are reasonably likely to have a material current or future effect on our financial condition, results of operations, liquidity or capital resources.

Indemnifications

In the ordinary course of business, we enter into contractual arrangements under which we may agree to indemnify the counter-party from losses relating to a breach of representations and warranties, a failure to perform certain covenants, or claims and losses arising from certain external events as outlined within the contract, which may include, for

example, losses arising from litigation or claims relating to past performance. Such indemnification clauses may not be subject to maximum loss clauses. We have also entered into indemnification agreements with our officers and directors. No material amounts related to these indemnifications are reflected in our consolidated financial statements for the years ended December 31, 2018, 2017 or 2016.

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Recent Accounting Pronouncements

See Note 1 to the consolidated financial statements in Item 15 of this report for a full description of recent accounting pronouncements.

Item 8. Financial Statements and Supplementary Data

Reference is made to the consolidated financial statements listed under the heading (a) (1) Consolidated Financial Statements and Report of Independent Registered Public Accounting Firm of Item 15, which consolidated financial statements are incorporated by reference in response to this Item 8.

Item 9. Changes in and Disagreements with Accountants on Accounting and Financial Disclosure

None.

Item 9A. Controls and Procedures

Evaluation of Disclosure Controls and Procedures

Under the supervision and with the participation of our management, including our Chief Executive Officer and Chief Financial Officer, we conducted an evaluation of the effectiveness of the design and operation of our disclosure controls and procedures, as defined in Rules 13a-15(e) and 15d-15(e) under the Securities Exchange Act of 1934. Based on this evaluation, our management concluded that as of December 31, 2018, our disclosure controls and procedures were effective.

Management’s Annual Report on Internal Control over Financial Reporting

Our management is responsible for establishing and maintaining adequate internal control over financial reporting, as such term is defined in Rules 13a-15(f) and 15d-15(f) under the Securities Exchange Act of 1934. In designing and evaluating the disclosure controls and procedures, management recognizes that any controls and procedures, no matter how well designed and operated, can provide only reasonable assurance of achieving the desired control objectives, and management necessarily is required to apply its judgment in evaluating the cost-benefit relationship of possible controls. Under the supervision and with the participation of our management, including our Chief Executive Officer and Chief Financial Officer, we conducted an evaluation of the effectiveness of our internal control over financial reporting based on the framework in Internal Control—Integrated Framework (2013 Framework) issued by the Committee of Sponsoring Organizations of the Treadway Commission. Based on the evaluation, our management concluded that our internal control over financial reporting was effective as of December 31, 2018.

Changes in Internal Control over Financial Reporting

There were no changes in our internal controls over financial reporting during the fourth fiscal quarter of 2018 that have materially affected, or are reasonably likely to materially affect, our internal control over financial reporting.

Item 9B. Other Information

None.

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Part III

Item 10. Directors, Executive Officers and Corporate Governance

The names of our directors and certain information about each of them are set forth below.

Name	Age	Position(s) with the Company
Daniel Lewis	70	President and Chief Executive Officer
Scott Lewis(1)	63	Director
Robert Y. Newell(1)(2)	70	Director
Daniel J. O'Neil(1)(2)	48	Director

(1) Member of Audit Committee
(2) Member of Compensation Committee

The principal occupations and positions for at least the past five years of our directors are described below. There are no family relationships among any of our directors or executive officers.

Daniel Lewis. Mr. Lewis was appointed to our board of directors in September 2017, and has served as our president and chief executive officer since August 2018. He has served as the managing member and an owner of GMS Manufacturing Solution LLC, which provides engineering services to manufacturing companies, since 2013. From 2001 to 2013, Mr. Lewis served as chief executive officer of View Box Group, LLC, which provides management consulting services to small businesses. Prior to 2001, he served as vice president of worldwide sales at both Xicor, Inc. and Integrated Device Technology, Inc. Mr. Lewis has also held various sales and technical positions with Accelerant Networks, Inc. Intel Corporation, Zilog, Inc. and Digital Equipment Corporation. Mr. Lewis holds a B.S. in Electrical Engineering from the University of Michigan. We believe that Mr. Lewis's qualifications to serve on the board of directors include his extensive business experience, having held senior management positions at several companies in the semiconductor, computer and networking industries. He brings strategic and operational insight to the board of directors.

Scott Lewis. Mr. Lewis was appointed to our board of directors in October 2018. He brings more than 40 years of design, sales, and product and corporate marketing experience with technology and semiconductor companies. He is not related to our chief executive officer. Since February 2018, Mr. Lewis has been serving as executive marketing strategist at United Silicon Carbide, Inc., a leader in the silicon carbide power device market. Previously, he held multiple corporate and product-line marketing leadership positions at Maxim Integrated Products, Inc., Global Foundries, Ltd., Cadence Design Systems, Inc., Intersil Corp., Xilinx, Inc. and Integrated Device Technology, Inc. Mr. Lewis holds a B.S. in Electrical Engineering Technology from DeVry Institute of Technology. We believe that Mr. Lewis's qualifications to serve on the board of directors include his extensive business experience with over 40 years of design, sales, product and corporate marketing experience in high-technology industries, primarily in management positions at several companies in the semiconductor industry. He also can provide the board with valuable insight into sales and customer management relevant to our business.

Robert Y. Newell. Mr. Newell was appointed to our board of directors in October 2018. He is currently a consultant and advisor to emerging technology and healthcare companies, having held financial management positions with technology and healthcare companies in Silicon Valley for over 25 years. From 2003 to 2018, Mr. Newell was CFO of

Dextera Surgical Inc., a developer of advanced stapling devices and automated medical systems. In December 2017, after entering into an agreement to sell substantially all of its assets, Dextera Surgical, Inc. filed a voluntary petition for reorganization under Chapter 11 of Title 11 of the United States Code in the United States Bankruptcy Court for the District of Delaware. Mr. Newell served on the board of directors of ARI Network Services, Inc., a leading supplier of SaaS and data-as-a-service solutions, from 2012 to 2017. Previously, Mr. Newell served as CFO of Omnicell, Inc., a hospital supply and medication management company, and held executive positions with the Beta Group, LLC and Cardiometrics, Inc. Prior to his business career, he was a pilot in the United States Air Force. Mr. Newell holds a BA in mathematics from the College of William & Mary and an MBA from Harvard Business School. We believe that Mr. Newell's qualifications to serve on the board of directors include his substantial financial and public-company experience, as he has served as chief financial officer at multiple medical device and other technology companies. He also has previous experience serving as a director on public-company boards of directors.

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Daniel O'Neil. Mr. O'Neil was appointed to our board of directors in September 2017 and has served as a partner at Acme Strategy, LLC, a provider of strategic consulting and advisory services, which he founded, since 2010. From 2008 to 2010, he served as an investment banker at Signal Hill Capital Group LLC. Prior to 2008, Mr. O'Neil held business development and investment banking positions at Energy Services Group, Deutsche Bank AG and BT Alex. Brown. Mr. O'Neil holds an AB from Harvard College and an MBA from the Stanford University Graduate School of Business. We believe that Mr. O'Neil's qualifications to serve on the board of directors include his extensive business experience and expertise in corporate finance and strategy, including experience gained both as an investment banker and corporate executive focused on the semiconductor and electronics industries. In the past, Mr. O'Neil has provided financial advisory services to us. He also brings to our board extensive knowledge of the semiconductor industry, along with deep experience in transactional processes, mergers and acquisitions, and deal financing for a wide range of transactions.

The names of our executive officers and certain information about them are set forth either above or below, as the case may be:

Name	Age	Position(s) with the Company
Daniel Lewis	70	President and Chief Executive Officer
James W. Sullivan	50	Vice President of Finance and Chief Financial Officer

James W. Sullivan. Mr. Sullivan became our Vice President of Finance and Chief Financial Officer in January 2008. From July 2006 until January 2008, Mr. Sullivan served as Vice President of Finance and Chief Financial Officer at Apptera, Inc., a venture-backed company providing software for mobile advertising, search and commerce. From July 2002 until June 2006, Mr. Sullivan was the Chief Financial Officer at 8x8, Inc., a provider of voice-over-internet-protocol communication services. Mr. Sullivan's prior experience includes various positions at 8x8, Inc. and PricewaterhouseCoopers LLP. He received a Bachelor of Science degree in Accounting from New York University and is a certified public accountant.

Section 16(a) Beneficial Ownership Reporting Compliance

Section 16(a) of the Exchange Act requires our directors, executive officers and persons who own more than 10% of a registered class of our equity securities to file with the SEC initial reports of ownership and reports of changes in ownership of common stock and other equity securities of ours. Directors, executive officers and greater than 10% holders are required by SEC regulation to furnish us with copies of all Section 16(a) reports they file. Based solely on our review of Forms 3 and 4 filed during 2018 (and any written representations to us by such persons), we believe that all directors, executive officers and 10% stockholders complied with all applicable Section 16(a) filing requirements during 2018 except that:

- Scott Lewis failed to timely file a Form 3 to register as a reporting person in October 2018.

Code of Ethics

We have adopted a code of ethics that applies to all of our employees. The code of ethics is designed to deter wrongdoing and to promote, among other things, honest and ethical conduct, full, fair, accurate, timely, and understandable disclosures in reports and documents submitted to the SEC and other public communications, compliance with applicable governmental laws, rules and regulations, the prompt internal reporting of violations of

the code to an appropriate person or persons identified in the code and accountability for adherence to such code.

The code of ethics is available on our website, www.mosys.com. We will provide to any person without charge, upon request, a copy of our code of ethics. Such a request can be made by contacting us via telephone at 408.418.7500 or via mail addressed to MoSys, Inc., 2309 Bering Drive, San Jose, CA 95131, attention: Corporate Secretary. If we make any substantive amendments to the code of ethics or grant any waiver, including any implicit waiver, from a provision of the code to our Chief Executive Officer or Chief Financial Officer, or persons performing similar functions, where such amendment or waiver is required to be disclosed under applicable SEC rules, we intend to disclose the nature of such amendment or waiver on our website.

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Audit Committee

Our board of directors established the Audit Committee for the purpose of overseeing the accounting and financial reporting processes and audits of our financial statements. The Audit Committee also is charged with reviewing reports regarding violations of our code of ethics and complaints with respect thereto, and internal control violations under our whistleblower policy are directed to the members of the Audit Committee. The responsibilities of our Audit Committee are described in the Audit Committee Charter adopted by our board of directors, a current copy of which can be found on the investors section of our website, www.mosys.com.

Scott Lewis, Daniel J. O'Neil, and Robert Y. Newell are the current members of the Audit Committee. All are independent, as determined in accordance with Rule 5605(a)(2) of the Nasdaq listing rules and Rule 10A 3 of the Securities Exchange Act of 1934, as amended (the "Exchange Act"). Mr. O'Neil serves as the chairman and has been designated by the board of directors as the "audit committee financial expert," as defined by Item 407(d)(5) of Regulation S K under the Securities Act of 1933, as amended, and the Exchange Act. That status does not impose on him duties, liabilities or obligations that are greater than the duties, liabilities or obligations otherwise imposed on him as a member of the Audit Committee and the board of directors, however. The Audit Committee has delegated authority to Mr. O'Neil for review and approval of non-audit services proposed to be provided by our independent registered public accounting firm.

Item 11. Executive Compensation

The information presented below has been modified to reflect the impact of a 1-for-10 reverse stock split effected in February 2017. See Note 1 of the consolidated financial statements in Item 15 of this Report for further discussion of the reverse stock split.

Compensation Committee

Robert Y. Newell and Daniel J. O'Neil are the current members of the Compensation Committee, with Mr. Newell serving as the chairman. The Compensation Committee is responsible for reviewing, recommending and approving our compensation policies and benefits, including the compensation of all of our executive officers and directors. Our Compensation Committee also has the principal responsibility for the administration of our equity incentive and stock purchase plans and the approval of equity awards to the named executive officers. The responsibilities of our Compensation Committee are described in the Compensation Committee Charter adopted by our board of directors, a current copy of which can be found on the investors section of our website, www.mosys.com.

Overview of Compensation Program

The Compensation Committee of the board of directors has responsibility for establishing, implementing and monitoring adherence to our compensation philosophy. The board of directors has delegated to the Compensation Committee the responsibility for determining our compensation policies and procedures for senior management, including the named executive officers, periodically reviewing these policies and procedures, and making recommendations concerning executive compensation to be considered by the full board of directors, when such approval is required under any of our plans or policies or by applicable laws.

The compensation received by our named executive officers in fiscal year 2018 is set forth in the Summary Compensation Table, below. For 2018, the named executive officers included Leonard Perham, President and Chief Executive Officer until his resignation in August 2018, Daniel Lewis, President and Chief Executive Officer effective

August 2018, James Sullivan, Vice President of Finance and Chief Financial Officer, and John Monson, Vice President of Marketing and Sales until his resignation in October 2018.

Compensation Philosophy

In general, our executive compensation policies are designed to recruit, retain and motivate qualified executives by providing them with a competitive total compensation package based in large part on the executive's contribution to our financial and operational success, the executive's personal performance and increases in stockholder value, as measured by the price of our common stock. We believe that the total compensation paid to our executives should be fair, reasonable and competitive.

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We seek to have a balanced approach to executive compensation with each primary element of compensation (base salary, variable compensation and equity incentives) designed to play a specific role. Overall, we design our compensation programs to allow for the recruitment, retention and motivation of the key executives and high level talent required in order for us to:

- supply high value and high quality integrated circuit solutions to our customer base;
- achieve or exceed our annual financial plan and be profitable;
- make continuous progression towards achieving our long term strategic objectives to be a high growth company with growing profitability; and
- increase our share price to provide greater value to our stockholders.

Role of Executive Officers in Compensation Decisions

The chief executive officer (CEO) makes recommendations for equity and non equity compensation for executives to be approved by the Compensation Committee. The Compensation Committee reviews these guidelines annually. The CEO annually reviews the performance of our executives (other than himself) and presents his recommendations for proposed salary adjustments, bonuses and equity awards to the Compensation Committee once a year. In its discretion, the Compensation Committee may accept, modify or reject the CEO's recommendations. The Compensation Committee evaluates the compensation of the CEO on its own without the participation or involvement of the CEO. Only the Compensation Committee and the board of directors are authorized to approve the compensation for any named executive officer. Compensation of new executives is based on hiring negotiations between the individuals and our CEO and/or Compensation Committee.

Elements of Compensation

Consistent with our compensation philosophy and objectives, we offer executive compensation packages consisting of the following three components:

- base salary;
- annual incentive compensation; and
- equity awards.

In each fiscal year, the Compensation Committee determines the amount and relative weighting of each component for all executives, including the named executive officers. Base salaries are paid in fixed amounts and thus do not encourage risk taking. Our widespread use of long term compensation consisting of stock options and restricted stock units (RSUs) focuses recipients on the achievement of our longer term goals and conserves cash for other operating expenses. For example, the RSUs granted to our executives in 2017 vest in increments over one and one-half years and will fully vest in 2019, and the stock options and RSUs granted to our non executive employees generally vest in increments ranging from 18 months to 36 months from the date of grant. The Compensation Committee does not believe that these awards encourage unnecessary or excessive risk taking because the ultimate value of the awards is tied to our stock price, and the use of multi year vesting schedules helps to align our employees' interests even more closely with those of our long term investors.

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Base Salary

Because our compensation philosophy stresses performance-based awards, base salary is intended to be a smaller portion of total executive compensation relative to long-term equity. The Compensation Committee takes into account the executive's scope of responsibility and significance to the execution of our long-term strategy, past accomplishments, experience and personal performance and compares each executive's base salary with those of the other members of senior management. The Compensation Committee may give different weighting to each of these factors for each executive, as it deems appropriate. The Compensation Committee did not retain a compensation consultant or determine a compensation peer group for 2018. In August 2018, upon the recommendation of Mr. Perham, our previous chief executive officer, the Compensation Committee authorized a base salary of $250,000 for Mr. Lewis on connection with his appointment as our new chief executive officer In September 2018, upon the recommendation of Mr. Lewis, the Compensation Committee awarded Mr. Sullivan a 1.2% increase in annual base salary, retroactive to July 1, 2017, thereby increasing his salary to $250,000. Mr. Sullivan had previously received a salary increase in 2017. The Compensation Committee determined that the increase was warranted based on the executive's performance and increases in the cost of living.

Annual Incentive Compensation

In September 2017, the Compensation Committee implemented a bonus plan for Messrs. Sullivan and Monson providing for bonuses of 15% and 5%, respectively, of their base salary. The Compensation Committee determined that these bonuses were warranted based on the executives' performance and increases in the cost of living, as the executives did not receive any salary increases in 2016. These bonuses were paid during 2017 and 2018.

In November 2018, the Compensation Committee authorized a bonus for Mr. Sullivan of 20% of his base salary. The Compensation Committee determined that this bonus was warranted based on Mr. Sullivan's performance.

Equity Awards

Although we do not have a mandated policy regarding the ownership of shares of common stock by officers and directors, we believe that granting equity awards to executives and other key employees on an ongoing basis gives them a strong incentive to maximize stockholder value and aligns their interests with those of our other stockholders on a long-term basis. The Equity Plan enables us to grant equity awards, as well as other types of stock-based compensation, to our executive officers and other employees. The Compensation Committee reviews and approves all equity awards granted under the Equity Plan to the named executive officers. We grant equity awards to achieve retention and motivation:

- upon the hiring of key executives and other personnel;
- annually, when we review progress against corporate and personal goals; and
- when we believe that competitive forces or economic conditions threaten to cause our key executives to lose their motivation and/or where retention of these key executives is in jeopardy.

With the Compensation Committee's approval, we grant options to purchase shares of common stock when we initially hire executives and other employees, as a long-term performance incentive. The Compensation Committee has determined the size of the initial option grants to newly hired executives with reference to option grants held by existing executives, the percentage that such grant represents of our total shares outstanding and hiring negotiations with the individual. In addition, the Compensation Committee would consider other relevant information regarding the size and type of compensation package considered necessary to enable us to recruit, retain and motivate the executive.

Typically, when we hire an executive, the options vest with respect to one-fourth of the total number of shares subject to the grant on the first anniversary of the grant date and with respect to 1/48th of the shares monthly thereafter. The options granted to executives in connection with annual performance reviews typically vest monthly over a three-to-four-year period, and RSUs granted typically vest annually over a period of from one-to-three years, as the Compensation Committee may decide. As matters of policy and practice we grant stock options with an exercise price equal to fair market value, although the Equity Plan allows us to use a different exercise price. In determining fair market value, we use the closing price of the common stock on the Nasdaq CM, on the grant date.

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Historically, no employee has been eligible for an annual performance grant until the employee has been employed for at least six months. Annual performance reviews are generally conducted in the first half of each fiscal year. Our CEO conducts the performance review of all other executives, and makes his recommendations to the Compensation Committee. The Compensation Committee also reviews the CEO's annual performance and determines whether he should receive additional equity awards. Aside from equity award grants in connection with annual performance reviews, we do not have a policy of granting additional awards to executives during the year. The board of directors and Compensation Committee have not adopted a policy with respect to setting the dates of award grants relative to the timing of the release of material non-public information. Our policy with respect to prohibiting insider trading restricts sales of shares during specified black-out periods, including at all times that our insiders are considered to possess material non-public information.

In determining the size of equity awards in connection with the annual performance reviews of our executives, the Compensation Committee takes into account the executive's current position with and responsibilities to us, and current and past equity awards to the executive.

While only the board of directors or the Compensation Committee may approve options or other equity-based compensation to our executives, the board of directors has authorized the CEO to approve option grants to employees at the senior director level and below for the purchase of not more than 100,000 shares by any employee during any calendar year. All such grants must be consistent with equity incentive guidelines approved by the Compensation Committee. The exercise price for such grants must be equal to the closing price of a share of the common stock on the Nasdaq CM on the date of grant.

Going forward, we intend to continue to evaluate and consider equity grants to our executives on an annual basis. We expect to consider potential equity awards for executives at the same time as we annually review our employees' performance and determine whether to award grants for all employees.

Accounting and Tax Considerations

Our Compensation Committee has reviewed the impact of tax and accounting treatment on the various components of our executive compensation program. Section 162(m) of the Internal Revenue Code (the "Code") generally disallows a tax deduction to publicly-held companies for compensation paid to "covered" executive officers, to the extent that compensation paid to such an officer exceeds $1 million during the taxable year. The Tax Cuts and Jobs Act repealed the performance-based exception to the deduction limit for remuneration that is deductible in tax years commencing after December 31, 2017. However, certain remuneration is specifically exempt from the deduction limit under a transition rule to the extent that it is "performance-based," as defined in Section 162(m) of the Code, and subject to a "written binding contract" in effect as of November 2, 2017 that is not later modified in any material respect. We endeavor to award compensation that will be deductible for income tax purposes, though other factors will also be considered. None of the compensation paid to our covered executive officers for the year ended December 31, 2018 that would be taken into account for purposes of Section 162(m) exceeded the $1 million limitation for 2018. Because of ambiguities and uncertainties as to the application and interpretation of Section 162(m) of the Code and the regulations issued thereunder, including the uncertain scope of the transition relief under the Tax Cuts and Jobs Act, no assurance can be given that compensation intended to satisfy the requirements for exemption from Section 162(m) of the Code in fact will satisfy such requirements. Our Compensation Committee may authorize compensation payments that do not comply with the exemptions to Section 162(m) when we believe that such payments are appropriate to attract and retain executive talent.

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Say-on-Pay

In 2017, we gave our stockholders an opportunity to provide feedback on our executive compensation through an advisory vote at our annual stockholder meeting. Stockholders were asked to approve, on an advisory basis, the compensation paid to our named executive officers. A majority of stockholders indicated approval of the compensation of the named executive officers, with approximately 90% of the shares that voted on such matter voting in favor of the proposal. Additionally, stockholders were asked to approve, on an advisory basis, in favor of having a stockholder vote to approve the compensation of the Company's named executive officers every three years. A majority of stockholders indicated approval of having a stockholder vote to approve the compensation of the Company's named executive officers every three years, with approximately 60% of the shares that voted on such matter voting in favor of the proposal. Based on these results and consistent with the previous recommendation and determination of its board of directors, the Company will hold non-binding advisory votes on executive compensation every three years until the next vote on the frequency of the stockholder advisory vote on executive compensation.

In light of the results of the advisory vote, the Compensation Committee has continued to apply principles that were substantially similar to those applied historically in determining compensation policies and decisions and did not make any significant changes to executive compensation decisions and policies with respect to 2018 executive compensation.

SUMMARY COMPENSATION TABLE

The following table sets forth compensation information for fiscal years 2018 and 2017 for each of our named executive officers.

Name and principal position	Year	Salary ($)	Stock Option Awards ($)(1)	Restricted Stock Awards ($)(1)	Non-Equity Incentive Plan Compensation ($)	Total ($)
Leonard Perham(2)	2018	101,446	—	—	—	101,446
Chief Executive Officer & President	2017	150,000	—	—	—	150,000
Daniel Lewis	2018	99,432	3,350 (3)	23,200 (3)		125,982
Chief Executive Officer & President						—
James Sullivan	2018	248,496	—	—	56,175 (5)	304,671
Chief Financial Officer & Vice President of Finance	2017	240,990	—	32,200	37,050 (5)	310,240
John Monson(4)	2018	194,989	—	—	25,000 (4)	
Vice President of Marketing & Sales					5,644 (5)	225,633

	2017	225,750	—	32,200	45,600	(4)	
					11,288	(5)	314,838

(1) Award amounts reflect the aggregate grant date fair value with respect to awards granted during the years indicated, as determined pursuant to FASB ASC Topic 718. The assumptions used to calculate the aggregate grant date fair value of option and stock awards are set forth in the notes to the consolidated financial statements included in item 15 of this Report. These amounts do not reflect actual compensation earned or to be earned by our named executive officers.

(2) Mr. Perham resigned as our president and chief executive officer in August 2018.

(3) Granted in his capacity as a director, prior to his hire as our chief executive officer in August 2018.

(4) Mr. Monson earned the amounts listed for him in the non-equity incentive plan compensation column for performance pursuant to a sales incentive plan. He resigned as our vice president of sales and marketing in October 2018

(5) Earned as bonuses in 2017 and 2018, as indicated.

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GRANTS OF PLAN-BASED AWARDS

We did not grant plan-based awards in 2018 to our named executive officers.

OUTSTANDING EQUITY AWARDS AT FISCAL YEAR-END

The following table sets forth information regarding the outstanding equity awards held by our named executive officers as of December 31, 2018.

	Option Awards					Stock Awards	
Name	Number of Securities Underlying Unexercised Options (#) Exercisable	Number of Securities Underlying Unexercised Options (#) Unexercisable	Equity Incentive Plan Awards: Number of Securities Underlying Unexercised Unearned Options (#)	Option Exercise Price($)	Option Expiration Date(1)	Number of Units That Have Not Vested (#)	Market Value of Units That Have Not Vested ($)
Daniel Lewis	26,667 (2)	53,333	—	0.75	10/19/2023	—	—
	6,667 (3)	13,333	—	1.28	1/4/2024	—	—
	—	—	—	—	—	20,000 (4)	3,326 (5)
James Sullivan	6,000 (6)	—	—	20.50	3/30/2025	—	—
	—	—	—	—	—	3,333 (7)	554 (5)
	12,277 (8)	3,508	—	7.20	8/23/2026	—	—
	—	—	—	—	—	11,666 (9)	1,940 (5)

(1) The standard option term is generally six to ten years, but all of the options expire automatically unless exercised within 90 days after the cessation of service as an employee, director or consultant.

(2) The stock option was granted on October 19, 2017 for service as a non-employee director, and the shares subject to this option vest annually over three years beginning September 26, 2018 subject to continued employment (or service as a director or consultant).

(3) The stock option was granted on January 4, 2018 for service as a non-employee director, and the shares subject to this option vest annually over three years beginning September 26, 2018 subject to continued service as an

employee, director or consultant.

(4) The shares subject to each restricted stock unit grant vest on February 1, 2019 subject to continued employment (or service as a director or consultant)

(5) The amount is calculated using the Company's closing price of $0.1663 per share of common stock on December 31, 2018.

(6) The stock option was granted on March 30, 2015, and the shares subject to this option vest monthly over 48 months subject to continued employment (or service as a director or consultant).

(7) The shares subject to each restricted stock unit grant vest annually over a three-year period commencing on March 1, 2017 subject to continued employment (or service as a director or consultant).

(8) In August 2016, officers tendered their eligible options and received new options at a rate of 1 replacement option share for each 1.75 option shares tendered. The stock option was granted on August 23, 2016, and the shares subject to this option vest monthly over 48 months subject to continued employment (or service as a director or consultant).

(9) The shares subject to each restricted stock unit grant vest in three equal installments on January 31, 2018, July 31, 2018 and January 31, 2019 subject to continued employment (or service as a director or consultant).

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OPTION EXERCISES AND STOCK VESTED

The following table sets forth the number of shares acquired and aggregate dollar amount realized pursuant to the exercise of options and vesting of stock awards by our named executive officers during 2018.

	Option Awards		Stock Awards	
Name	Number of Shares Acquired on Exercise(#)	Value Realized on Exercise($)	Number of Shares Acquired on Vesting(#)	Value Realized on Vesting($)(1)